TEXAS INSTRUMENTS

RS-422 and RS-485 Interface Circuits

Data Transmission and Control Circuits

Application and Data Book

1992

Linear Products

Linear Products Quick Reference Guide

Data Book	Contents	Document No.
• Linear Circuits Vol 1 Amplifiers, Comparators, and Special Functions	Operational Amplifiers Voltage Comparators Video Amplifiers Hall - Effect Devices Timers and Current Mirrors Magnetic - Memory Interface Frequency - to - Voltage Converters Sonar Ranging Circuits/Modules Sound Generators	SLYD003, 1989
• Linear Circuits Vol 2 Data Acquisition and Conversion	A/D and D/A Converters DSP Analog Interface Analog Switches and Multiplexers Switched - Capacitor Filters	SLYD004, 1989
• Linear Circuits Vol 3 Voltage Regulators and Supervisors	Supervisor Functions Series - Pass Voltage Regulators Shunt Regulators Voltage References DC - to - DC Converters PWM Controllers	SLYD005, 1989
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• Speech System Manuals	TSP50C4X Family TSP50C10/11 Synthesizer TPS53C30 Synthesizer	SPSS010, 1990 SPSS011, 1990 SPSV003, 1990
• Interface Circuits	Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers	SLYD006, 1991
• Telecommunications	Transmission, Switching, Subscriber, Cicuits Transient Suppressors	SCTD001B, 1991
• Power Products	Transistors Darlingtons SCR's Triacs Transient Suppressors Lighting Starters	DB029,1990

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Section 1

General Information

Introduction

This booklet provides the design engineer with a single point of reference for data and application information concerning the two most popular differential communication standards, RS-422 and RS-485. The book contains information on many new products in addition to older industry standard parts.

The application information concentrates on two areas, information relating to the EIA standards, and device information on new products and how they help solve design problems. The new product evolution can be thought of as moving in three directions:

- **Higher Data Rates** for high speed applications such as differential SCSI.
- **Low Power** for higher reliability and remote applications.
- **Integration** where more than one transmission line is required.

TI is tackling all three of these areas with its new products by using innovative design techniques and Advanced technologies. For low power applications, LinBiCMOS with it's robust bipolar output structures is the ideal choice for Low Power applications. Where high speed is the critical factor, Advanced low power shottky achieves the highest data rates of any RS-485 transceiver, 35MBPS for the SN75ALS176B.

Selecting the Best Device for your application

In the first instance use the **selection guide** at the back of this section.

1. Decide whether you need a transceiver or driver/receiver configuration.

2. Decide how many drivers/receivers/transceivers are needed in your application.

3. Choose from the key features listing the key requirement for your application - specifically high speed, or low power.
4. Refer to the data sheet for final verification of device selection keeping in mind package options and temperature range options.

RS-422 Data Transmission Circuit Selection Guide

RS-422 Drivers

Devices Per Package	Device Part Number	Key Features	Page Number	
			Data Sheet	Application
2	SN75158	Industry Standard	3-76	-
	SN75159	Industry Standard	3-83	-
	SN75ALS191	High Speed	3-240	2-20
	uA9638	Industry Standard	3-319	-
4	AM26C31	Low Power	3-3	2-22
	AM26LS31	Industry Standard	3-12	2-20
	MC3487	Industry Standard	3-34	-
	SN75151	Industry Standard	3.60	-
	SN75153	Industry Standard	3-60	-
	SN75ALS172	High Speed	3-194	2-45
	SN75ALS174	High Speed	3-206	2-45
	SN75172	Industry Standard	3-94	2-45
	SN75174	Industry Standard	3-110	2-45
	SN75ALS192	High Speed	3-244	2-19
	SN75ALS194	High Speed	3-264	2-10

RS-422 Selection Guide (continued)

RS-422 Receivers

Devices Per Package	Device Part Number	Key Features	Page Number	
			Data Sheet	Appli-cation
2	SN75146	5 MHz LP I/P Filter	3-55	-
	SN75157	Industry Standard	3-71	-
	uA9637	Industry Standard	3-314	-
	uA9639	Industry Standard	3-323	-
4	AM26C32	Low Power	3-8	2-22
	AM26LS32	Industry Standard	3-20	2-22
	MC3486	Industry Standard	3-29	-
	SN75173	Industry Standard	3-102	2-45
	SN75175	Industry Standard	3-117	2-45
	SN75ALS173	High Speed	3-200	2-45
	SN75ALS175	High Speed	3-212	2-45
	SN75ALS193	High Speed	3-253	2-19
	SN75ALS195	High Speed	3-274	2-19

RS-422 Selection Guide (continued)

RS-422 Transceivers - Driver\Receiver Combination

Devices Per Package	Device Part Number	Key Features	Page Number	
			Data Sheet	Appli-cation
1	SN75176A	Low Power	3-125	2-14
	SN75176B	Industry Standard	3-135	2-14
	SN75177B	Repeater	3-145	2-46
	SN75178B	Repeater	3-145	2-46
	SN75ALS176	High Speed	3-218	2-10
	SN75ALS176A	Very High Speed	3-218	2-10
	SN75ALS176B	Ultra High Speed	3-218	2-10
	SN75LBC176	Ultra- Low Power	3-285	2-41
	TL3695	Industry Standard	3-303	2-15
1/1	SN75179B	Industry Standard	3-156	2-46
	SN75ALS180	Industry Standard	3-230	2-16
2/2	SN751177	High Speed	3-47	2-37
	SN751178	High Speed	3-47	2-37
3	SN75ALS170	High Speed	3-163	2-15
	SN75ALS171	High Speed	3-179	-

RS-485 Data Transmission Circuits Selection Guide

RS-485 Drivers

Devices Per Package	Device Part Number	Key Features	Page Number	
			Data Sheet	Appli-cation
4	SN75172	Industry Standard	3-94	2-45
	SN75174	Industry Standard	3-110	2-45
	SN75ALS172	High Speed	3-194	2-45
	SN75ALS174	High Speed	3-206	2-45

RS-485 Receivers

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	SN75175	Industry Standard	3-117	2-45
	SN75ALS173	High Speed	3-194	2-45
	SN75ALS175	High Speed	3-206	2-45

RS-485 Selection Guide (continued)

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3	SN75ALS170	High Speed	3-163	2-15
	SN75ALS171	High Speed	3-179	-

Section 2

RS-485 and RS-422 Application Guide

The Need for Balanced Transmission Line Standards

High speed data transmission between computer system components and peripherals over long distances, under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-422 and **RS-485** are balanced (differential) digital transmission line interfaces developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations. The advantages are;

- **Data rate - to l0 Mbps and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

Application Areas

RS-422 offers a reliable multi-point one way communication. A typical application area is its use in transmitting data from a central computer to multiple remote monitors, printers or stations, such as airport arrival and departure monitors.
RS-485 is an upgraded version of RS-422 extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bi-directional multi-point party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.
As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the electrical specification of their standard. Examples include the ANSI (†American Nationals Standards Institute) Small Computer Systems Interface (SCSI).

Differences between EIA RS-422-A and EIA RS-485

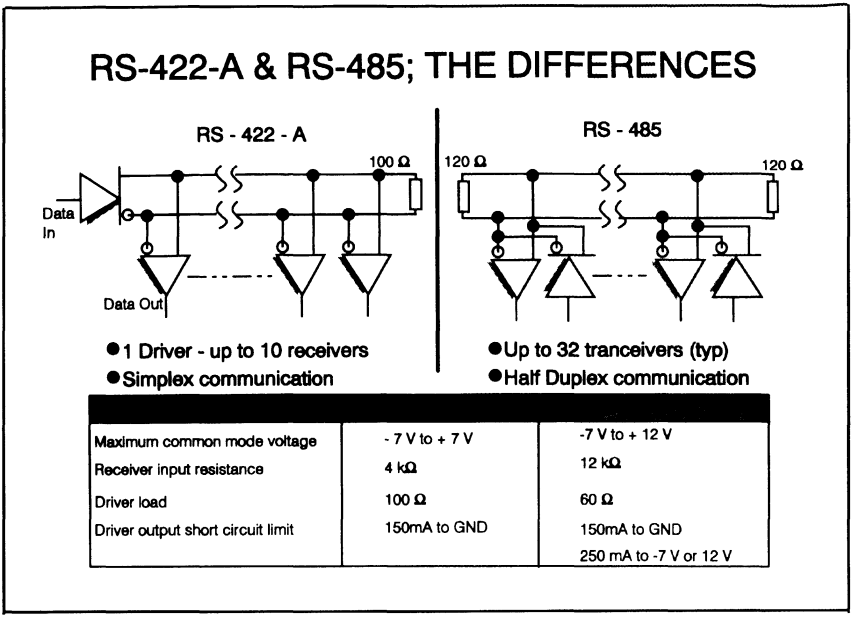


Figure 1 - EIA RS-422-A and EIA RS-485 Differences

EIA RS-422-A

The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS422A) in December 1978 bringing it in line with its present specifications.

A RS-422 line allows for only one way communication (simplex mode) but by using a differential twisted pair transmission media (not specified in std.) and a RS-422 receiver with its minimum 7 V common mode voltage capability makes it less susceptible to noise picked up in hostile environments, via the long cables allowed by the standard. Each driver can drive up to 10 receivers. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10 Mbps are supported and a line length up to 1200 metres is given as guide-line, but not at the maximum data rate.
When operating at low data rates (below 200 kbps), or at any speed where the ratio of the driver's output rise time to the one-way propagation delay time of the cable

exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line.

The characteristic impedance of twisted pair cable is a function of frequency and cable type, however typical twisted pair cable impedance's lie in the range of 100Ω to 120Ω. A termination resistor with an impedance similar to the cable's characteristic impedance should only be connected at the furthest end of the cable.

EIA RS-485

The Increased use of balanced data transmission lines in distributing data to several system components and peripherals over relatively long lines brought about the need for multiple driver/receiver combinations on a single twisted pair line. Hence, an upgraded version of EIA RS-422-A , named EIA RS-485, was introduced in 1983. RS-485 takes into account RS-422 requirements for balanced-line data transmission plus additional features allowing for multiple drivers and receivers. The guide-lines for data transmission speed, cable lengths and media are the same as for RS422.

The Differences

The differences between the RS-485 standard and the RS-422 standard lie primarily in the features that allow reliable multi-point communications.

Driver features

i. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

ii. The driver output, off-state, leakage current shall be 100 µA or less with any line voltage from -7 V to +12 V.

iii. The driver shall be capable of providing a differential output voltage of 1.5 V to 5 V with common-mode line voltages from -7 V to 12 V.

iv. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

Receiver features

i. High receiver input resistance, 12 kΩ minimum.

ii. A receiver input common-mode range of -7 V to 12 V.

iii. Differential input sensitivity of ±200 mV over a common-mode range of -7 V to 12 V.

EIA RS-485 /422 Product /Application Trends

Proprietory system designers are beginning to recognise the inherent advantages of a balanced, differential, transmission scheme over the single ended interface. Such advantages are higher noise immunity, lower noise emissions and improved signal quality. These facts are also not lost on independent standards committees which are starting to embrace RS-485 as the electrical part of their overall specification. Furthermore those systems not following the RS-485 specification verbatim are recognising the virtues of Texas Instruments range of differential driver/receivers, particularly the high speed/low power ALS options.

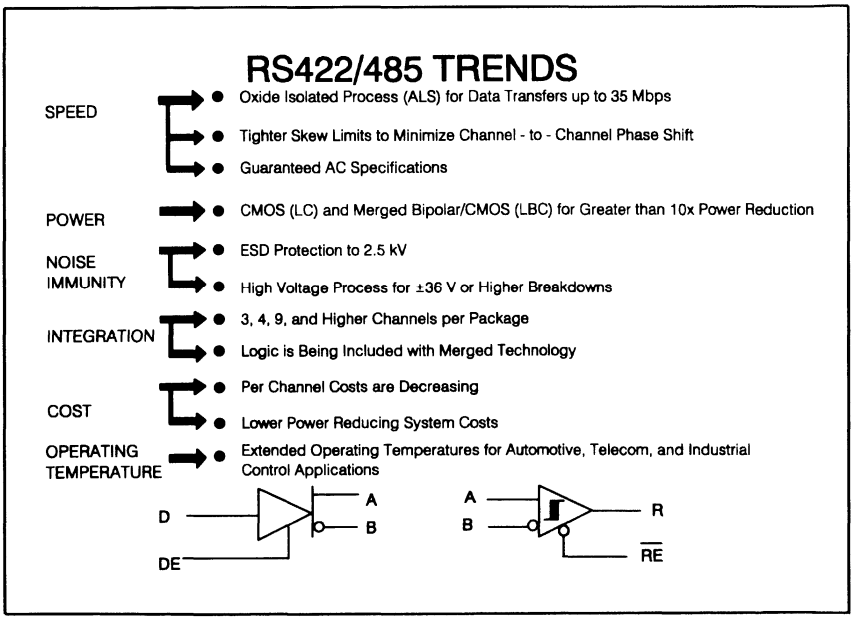


Figure 2 - EIA RS-485 /422 Product /Application Trends

Representatives of those standards bodies employing a differential transmission scheme can be found in most industries, some examples are listed below;

i) **Computer;** The ANSI-X3T9.2-1986 Small Computer Systems Interface (SCSI)

ii) **Computer;** ANSI X.3129-1986 Intelligent Peripheral Interface (IPI)

iii) **Automotive multiplex Wiring;** CAN, VAN and SAE J1850

iv) **Telecommunications;**

v) **Factory Automation;** P-Net (A derivative of Field bus)

Each one of these application areas makes its own demands on the processing technology used. Examples of these demands are guaranteed AC specifications and increased data rate capability. In particular, tighter skew specifications are needed for both telecommunication and computer applications, however the interpretation of skew can differ. For example, telecommunication applications are more concerned with device skew, that is the difference between the positive and negative edges of the differential output voltage. A low skew value in this case would represent a lower likelihood of noise radiation. For the computer application, SCSI, a low bus skew is required. In a SCSI there can be as many 18 differential lines, obviously for timing purposes it is desirable to have low skew between each channel. For these types of applications a high speed bipolar process like the advanced low power Schottky would be required.

A key requirement across most application areas is low power consumption, particularly with the emergence of battery backed or operated equipment. This requires a low power technology, for example CMOS. However although fine for controller applications, CMOS is not generally suitable for line drive / receive functions, here a more robust technology is needed, for example, a bipolar or merged technology like Texas Instruments LinBiCMOS (combination of analogue bipolar and analogue CMOS).

Due to the increasing use of differential systems, particularly in electrically hostile environments, increased common mode voltage ranges and low susceptibility to ESD (Electro-Static Discharge) damage is required. Furthermore, extended temperature ranges are required particularly in automotive applications where the line drive/receive functions may be located under the car bonnet (hood). All new devices in Texas Instruments range of line drivers and receivers contain temperature range options for both commercial, 0°C to 70°C and industrial, -40°C to 85°C. Some devices like the SN65076 have been designed especially for automotive applications by offering a - 40°C to 105°C temperature range.

One final demand made by all types of equipment is for increased integration. Designers are requiring increased functionality from semiconductor chips and, perhaps an even more importantly require that these chips be less expensive than the solution(s) they replace.

Differential Line Considerations

A differential communication system requires the use of two 'signal carrying' wires between driver and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the difference in voltage between the two wires. The absolute value of the dc common

mode voltage of the two wires is not important. In practice, drivers and receivers have a finite common mode voltage range within which they can operate.

The use of a differential communications interface allows data transmission at high rates and over long distances to be accomplished. This is because effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output voltage to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost, but provides superior performance when data is to be transmitted at high rates over a long distance.

Transmission Line Considerations and Effects

Before design of a digital data link can take place application constraints and an understanding of the signal's characteristics must be understood. More specifically, a method of identifying the class of data link, and any special design techniques required must be made.
A digital data link can be classed in two modes;

i) A transmission line (distributed parameter model)

ii) Short wire (lumped parameter model).

A distributed parameter model considers the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections making up the line. The result is that a transmission line is said to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a wave front at any point as it travels along the line.

The transmission line will always consist of two conductors, with the current flowing in opposite directions in each of the conductors. In the single ended case, one of these conductors is the ground wire.

The speed that a pulse travels at along a transmission line approaches that of the speed of light. The type of cable used will provide the limit to the actual speed.

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings. If the signal starts to change at the driver's output at one end of the line, the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the driver terminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system. A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the rise time , t_T, of the signal is much less than the round trip propagation delay, 2tpd, of the signal from driver to receiver and back to driver, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, tpd, to occur during the transition edge time.

When the cable is operating like a transmission line, extra loads in the form of drivers and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. The extra devices will decrease the line impedance and reduce the speed of the signal along the line.

In the case of the lumped parameter model, the line tends to represent a pure fixed load to the driver device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of a driver device that can supply a finite amount of current to the line.

Line Termination

It is generally good design practice to terminate the ends of lines which are classified as transmission lines. Here the golden rule is to match the impedance from the source of the driver to the characteristic impedance of the cable, and from the cable to the characteristic impedance of the receiver. If there is an impedance discontinuity at any junction, then the signal will be reflected from the mismatch. This will lead to signal distortion which in turn leads to either a falsely triggered receiver or excessive propagation delay. Calculation of a suitable value for this termination value will be dealt with later in this section whilst a more detailed discussion can be found in the transmission line fundamentals section at the front of the data transmission section.

Data Rate and Line Length Limitations

Most application areas will demand some kind of compromise between the line length used and the data rate required, particularly if distortion in its many guises is to be avoided. A first, all important, step in understanding what compromises are necessary is to recognise the various forms of distortion and why they occur.

No transmission line is perfect, even by sending current down the line some voltage drop will occur due to the resistive nature of the line, this in its most simplistic form is distortion. This is compounded when longer line lengths are used where the attenuation from source to destination can cause quite severe distortion. This places a limit on the line length even at low data rates. A typical cable of 24 SWG can have a series resistance of 80Ω per km, and so the line length will be limited to the order of 1200m (series resistance equals the line's characteristic impedance).

Other Effects

Other effects acting upon the transmission line are due to phase distortion introduced on the driver's transition edges. The high speed edges, necessary for high speed systems, have a high frequency harmonic content. The inductive and capacitive (and resistive) nature of the line introduces delay and distortion into these harmonics. This in turn reduces the clarity of the signal being sent down the line, thus increasing the probability of error.

This effect is normally measured using eye patterns which measure the jitter and distortion in the signal being sent down the line. It is this effect that causes the predominant reduction in data rate as the line length increases. Another limitation can be caused by incorrect termination of the line, causing reflections. These reflections can cause errors due to loss of timing information.

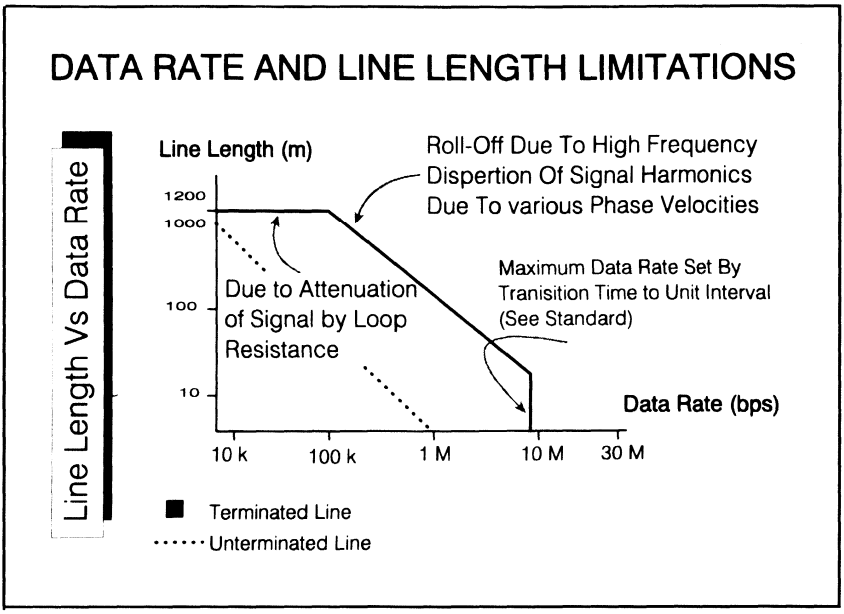


Figure 3 - Data Rate and Line Length Limitations

In conclusion, distortion and thus data integrity is a function of signal rise time and line attenuation. Signal rise time and attenuation are often quoted in manufactures data, and can be used to determine the line distortion.

RS-422/RS-485 Data Rate Definition

Another limitation of system performance are the speed limitations of the line driving elements themselves. No device, no matter what technology used, will have zero propagation delays and transition times. The trick is to ensure that any delay introduced by these devices is insignificant in comparison to the line propagation delay. To ensure the device does not introduce distortion, i.e. to maintain signal shape, it is good design practice to set a ratio between the unit interval, t_b, and the transition rise time, t_T. This limitation is often specified in the standard being used. For RS-422-A the ratio of t_T to t_b is 1:10, and for RS-485 1:3.

Note these calculations only give an indication of the drivers data rate capability, obviously the receivers propagation delay needs to be considered for the system data rate. Furthermore in multi channel systems the slowest driver and receiver in the system set the overall system data rate (see the differential ac specifications section following).

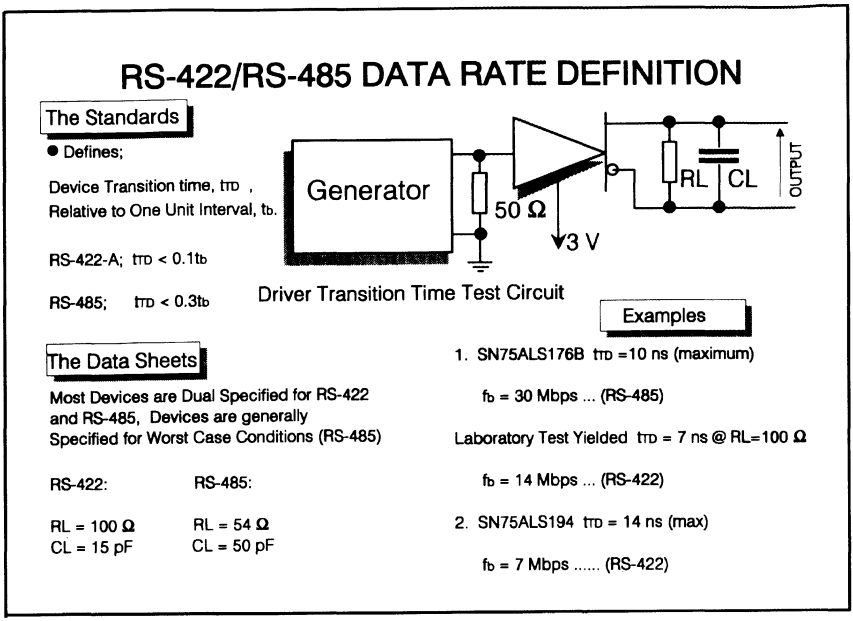


Figure 4 - RS-422/RS-485 Data Rate Definition

Many devices within the Texas Instruments range are specified for both RS-422 and RS-485 operation. The differing specifications of relating t_T to tb between the standards makes an understanding of data rate capability for RS-422 operation difficult to ascertain, since these devices are tested to the worst case conditions of the RS-485 specification. That is, the driver output is driven into a resistive load of 54Ω in parallel with a capacitive load of 50 pF.

An example of such a device is the SN75ALS176 which can be used for both RS-422 or RS-485.

Examples

1. **SN75ALS176B** has a differential-output transition time t_T of 10 ns(Max). Therefore; $t_b = 3.33 \times 10 \times 10^{-9} = 33.3$ ns giving a minimum theoretical frequency of **30 Mbps.**

As the data sheet specifies a minimum t_T = 5 ns the maximum theoretical data rate could be as high as 60 Mbps.

Using the RS-422 data rate test for this devices does not give a clear picture as the standard requires a lighter load to be applied. However, laboratory test using the RS-422 load gives a t_T for the ALS176 of 7 ns (RS-485 load = 14 ns) indicating a RS-422 data rate of 14 Mbps.

2. **SN75ALS194** has a differential-output transition time t_T = 14 ns(Max). Since this device is specified solely for RS-422 we can clearly calculate the minimum theoretical data rate.

Therefore; $t_b = 10 \times 14 \times 10^{-9} = 10 \times 14 \times 10^{-9}$ giving a minimum theoretical frequency of **7 Mbps.**

Again a more aggressive data rate could be achieved if the typical specified value for t_T = 8 ns was used. Giving a typical frequency of 12.5 Mbps.

Differential AC specifications

For multi channel systems, like SCSI, consideration of the drivers differential transition time is not sufficient to determine the systems data rate capability. More specifically the slowest driver/receiver within the system will usually set the limit.

Although much detail is contained within multi channel standards, such as the ANSI SCSI standard, concerning most aspects of the electrical interface, ac considerations are not. Many of these standards define the overall bus timing requirements but the budgeting of timing error contributions is left to the system designer.

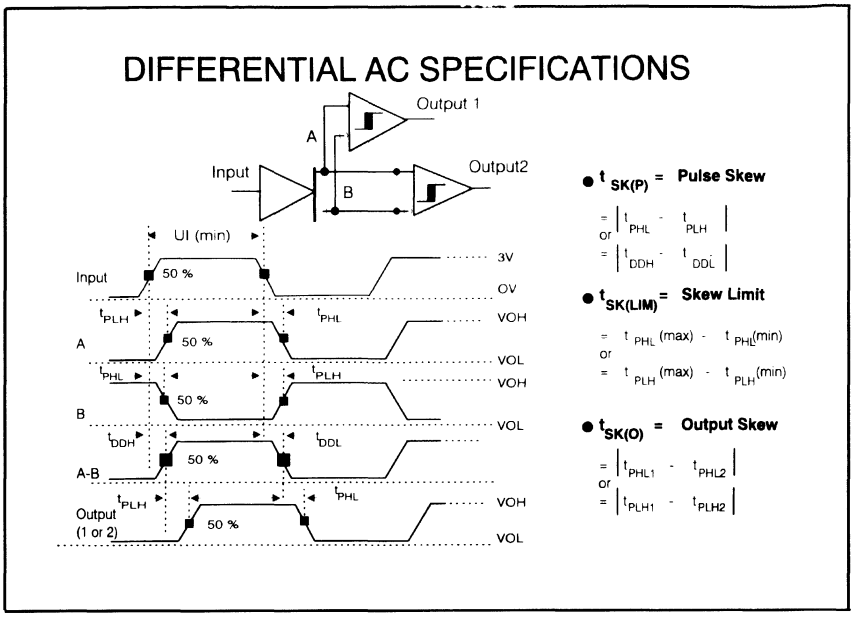


Figure 5 - Differential AC specifications

When driving the line at high speeds the effects of the driver and receiver on the system become more apparent. The magnitude of the driver and receiver propagation delays relative to the unit interval increase, causing asymmetries in the edges. These asymmetries have three main effects;

i. Decreased data rate capability

ii. Decreased noise immunity

iii. Increased risk of noise radiation

Figure 5 shows how these delays manifest themselves in a differential data transmission scheme.

A Discussion of Skew

There are many catagories of delay, termed skew, in a differential line system. This understanding is further complicated when you consider that a driver is really a single ended input to differential output converter, while the receiver is a differential input to single ended converter.

Skew measurements are either **propagational**, single ended (t_P), or **differential, single ended to differential** (t_{DD}).

Pulse Skew; ($t_{SK(P)}$)

Propagational Pulse skew ($t_{SK(P)}$) is measured between the 50% level of the input pulse and the 50% level of the driver single ended output pulse (either A or B in the figure). Differential pulse skew is measured between the 50% level of the input pulse and the 50% level of the driver differential output pulse (A-B).

In the ideal situation where $t_{PHL} = t_{PLH}$ or $t_{DDH} = t_{DDL}$, pulse skew effectively displaces the signal on the line in time, and no signal distortion should occur - although these delays will need to be allowed for when synchronising data in multi channel systems. However if the rise and fall time delays are not the equal then the resultant differential signal may become distorted. Typically this distortion will cause the differential signal to flatten out around the receivers transition region, i.e. at the common mode voltage of the line. As a result the system will have a lower noise immunity and increased likelihood of RFI radiation.

Propagation pulse skew or differential pulse skew may be specified for either drivers or receivers. Normally propagation pulse skew is specified in older driver data sheets whilst differential pulse skew, a more meaningful measurement, is specified on more modern devices. For example Texas Instruments SN75ALS176B, best in the industry, has a pulse skew of 2 ns.

Although the figure shows differential pulse skew measurement, production testing is usually carried out as a propagation skew measurement. This is due to the difficulties in generating a true differential signal. This parameter is tested with one input tied at a reference voltage and the other toggled, giving a single ended propagation delay.

Skew Limit; $t_{SK(LIM)}$

Skew limit is the greater of either the difference between the maximum and minimum specified values of t_{PLH} (or t_{DDL}) or the difference between the maximum and minimum specified values of t_{PHL} (or t_{DDL}). In effect this is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device-to-device. This is a particularly useful parameter for determining the data rates in multi-channel bus systems, since it sets a limit on signal delays between channel to channel.

Output Skew; $t_{SK(O)}$

This is simply the delay between the t_{PLH} or t_{PHL} receiver output levels within a multi-channel system.

Defining the Minimum Unit Interval (UImin)

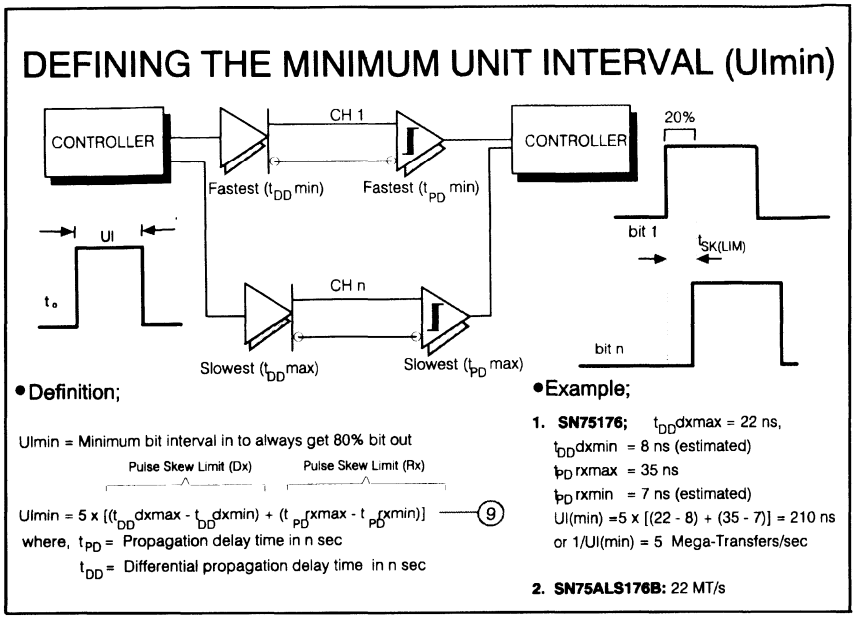


Figure 6 - Defining the Minimum Unit Interval (UImin)

Figure 6 shows the application of the skew limit test to a multi-channel system in order to calculate the maximum data rate capability, this is shown as equation 9. To maintain synchronisation and signal integrity there must be a minimum overlap between the signals on each channel. As a basic rule the skew limit must be no greater than 20% of the unit interval.

The calculations compare the data rate capability of the low power Schottky SN75176 to the advanced low power Schottky SN75ALS176,

SN75ALS176B High Speed Transceiver

Figure 7 (uses equation 9) to compare the data rates of various differential devices available from Texas Instruments. The fastest RS-485 compatible differential transceiver available today is the SN75ALS176B.

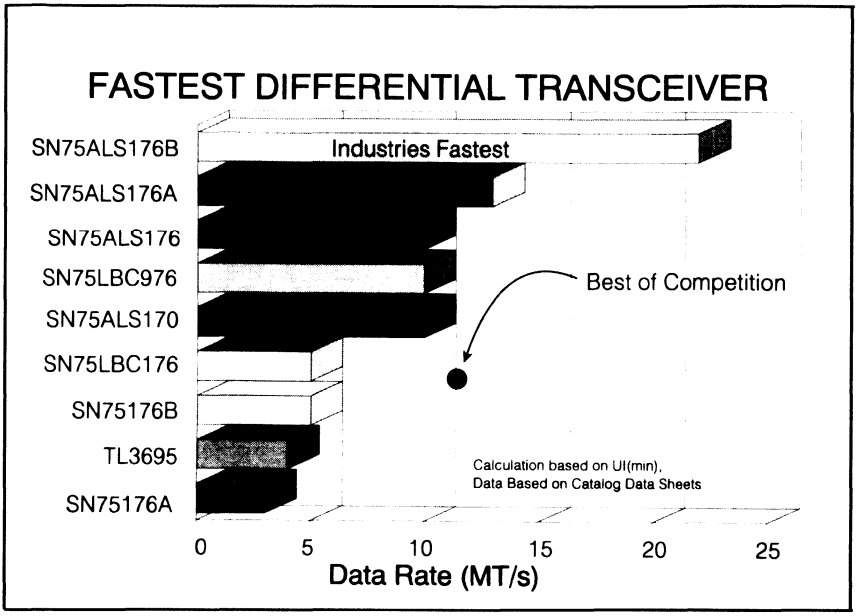


Figure 7 - Fastest Differential Transceiver

High Speed/Low Power Applications

The SN75ALS176 forms just part of a range of high performance single line driver/receiver options available for RS-422 and RS-485 applications. Some key benefits of this range are discussed in the following text.

The range of devices shown in the figure are all high speed low power monolithic integrated circuits, designed for bi-directional data communication on multi-point bus transmission lines. The SN65ALS176, SN75ALS176 series and TL3695 are single differential transceivers, while the SN65ALS180 and SN75ALS180 are a single differential driver/receiver pair.

All devices are designed for balanced transmission lines and meet EIA standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

The SN65ALS176, SN75ALS176 series and TL3695 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables,

respectively, which can be externally connected together to function as a direction control. The driver's differential outputs and the receiver's differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or VCC = 0V. This port features a wide positive and negative common-mode voltage range making the device ideal for party line applications. All devices are available in either 8-pin dual-in-line plastic (P) or 8-pin plastic small outline surface mount (D) packaging.

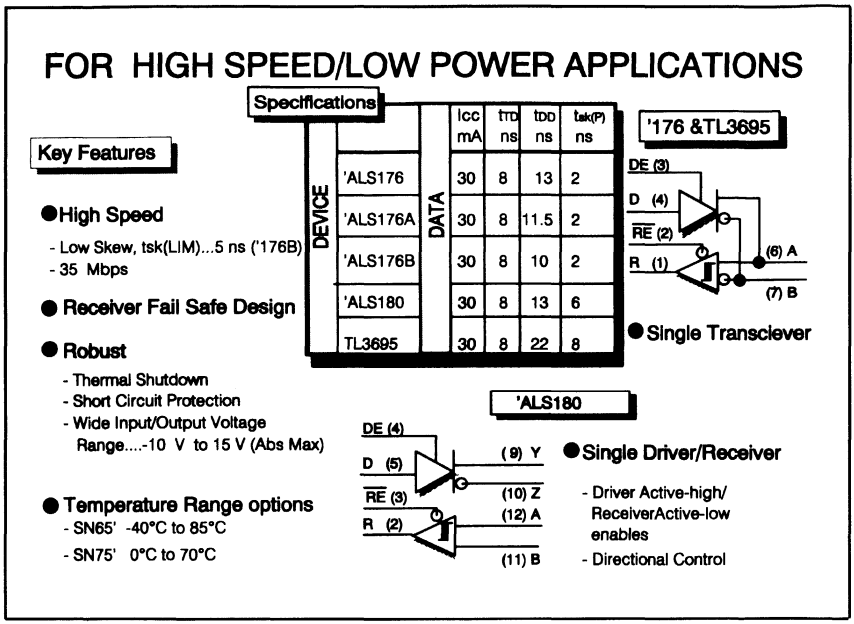


Figure 8 - For High Speed/Low Power Applications

The SN75ALS180 contains many of the same features listed above. However, the driver outputs and receiver inputs are not internally connected together but are brought outside the chip, offering a separate driver and receiver function. For this reason the SN65ALS180 and SN75ALS180 are housed in a 14-pin dual-in-line plastic and 14-pin small outline plastic packages. This arrangement makes the SN75ALS180 ideal for full duplex operation.

Product Differentiation

The SN75ALS176 series allows the designer to select between ac performance levels. The figure shows the maximum propagation delays and skew specification for the range. The SN75ALS176B offers the highest speed performance with a maximum

differential output delay time of 10†ns. With a minimum specified value of 5ns the device is capable of data rates in excess of 60 Mbps (as per RS-485 specification).
Perhaps even more importantly, especially for high speed multi-channel applications (for example SCSI), is the low skew value, $t_{sk(LIM)}$. In this instance skew is specified as the difference between the maximum and minimum differential output delay times, T_{DD}. The SN75ALS176B has a minimum $t_{sk(LIM)}$ value of 5ns. This value is used to determine the delays in signals between channels in the system. The pulse skew, $t_{sk(P)}$, is specified as a minimum value of 2ns (see previous discussion of skew).

The TL3695 provides the same functionality as the 'ALS76 series of devices, but is aimed at lower performance lower cost systems.

Low Skew And EMI

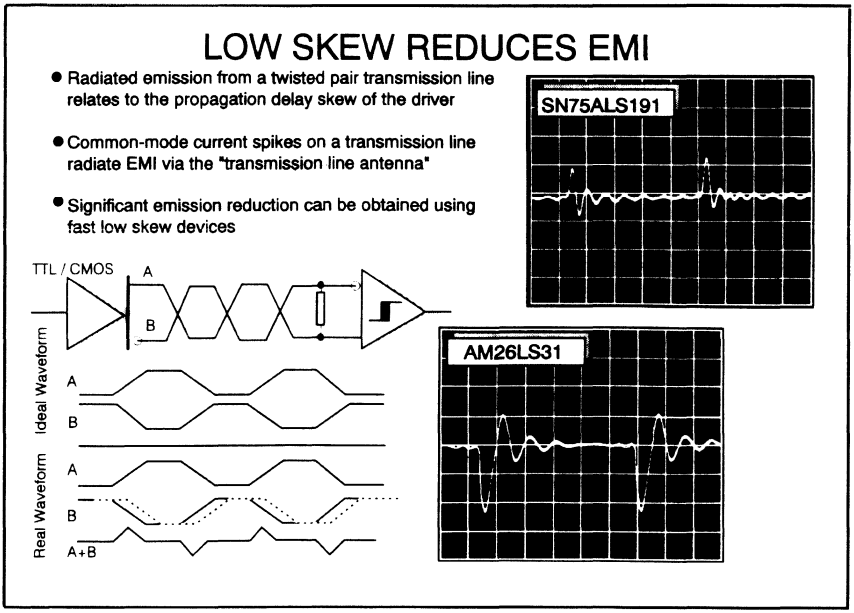


Figure 9 - Low Skew Reduces EMI

Further justification for low skew designs is set out in the following paragraphs;

EMI Related to Differential Transmission Lines

Radiated emissions from electronic systems has been receiving more attention as mutual disturbances between electronic equipment increase and the subsequent need for EMC regulations becomes more apparent. This is compounded by the increased use of high clock rates and high currents which generate high frequency EMI. Applications placed on printed circuit boards are normally enclosed in a confined space making the problem easier to solve, but when transmitting data signals to the outside world through cables, increasing the total radiated emission by the system is difficult to avoid.

In large computer systems, Inter-unit cables within the system have been found to be responsible for much of the radiated emission. Further studies have revealed that the noise itself is a function of common mode current spikes, brought about by the skew between the outputs of clocked differential drivers. Significant improvements in system-wide emissions were seen in practice after replacing high skew driver devices with others those which had less skew.

The effect seen is not only related to large computer systems but is saleable to all systems using differential transmission lines. Differential drivers and receiver are designed to operate under conditions with high common mode signals. Low frequency common mode signals usually cause no problems, but high frequency common mode spikes cause EMI and in systems with inter-unit cabling an antenna is readily available increasing the radiated emission. Clearly, twisted pair cables used to interconnect boards within the same cabinet, or to establish data transmission between various equipment, using for example the popular standards RS-422-A or RS-485, are likely to radiate EMI if the driver's complementary outputs are not exactly symmetrical. This is true for the single differential line in an industrial system as well as for the many parallel differential lines used in a SCSI interface cable.

Low Skew Devices Reduce EMI

Ideally, a differential driver should not generate common mode signals due to the nature of the differential output and the twisted cable cancelling the common-mode currents but in practice, small differences between the complementary outputs occur which produce fast common mode pulses on the line.

The skew specification, specified as the propagation delay difference from the input of the differential driver to the driver's respective inverting and non-inverting outputs is a good measure for how much or how little radiation that can be expected from high frequency common mode signals during switching. However, a low skew specification on its own does not guarantee negligible common mode signals as the signals can still be non symmetrical due to different rising and falling wave forms. In such cases Significant current spikes can be measured on the line.

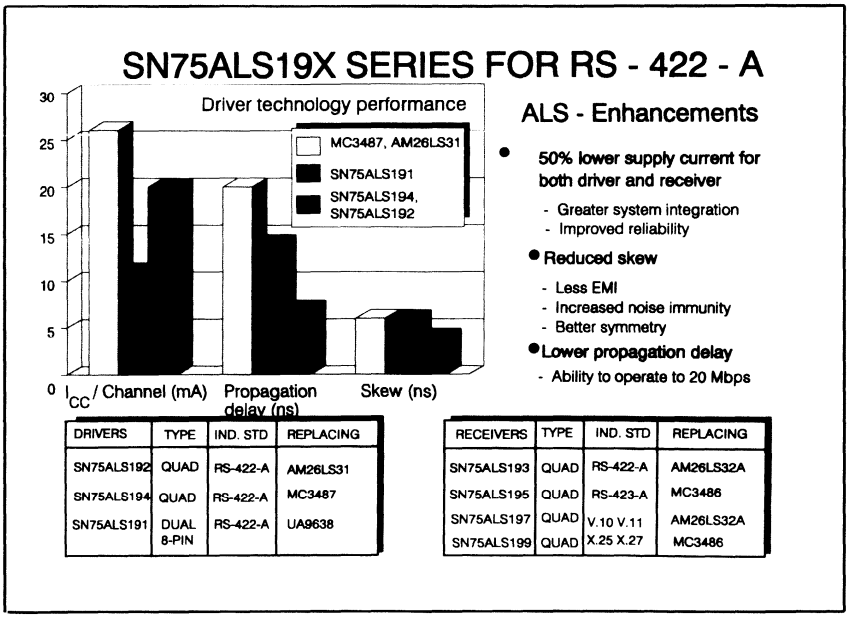
Use Fast Devices Even in Low Data Rate System

Even in systems where low data rates are used, EMI can still cause problems with EMC regulations. These problems are best solved by employing high speed devices usually having a significant lower skew than slower drivers.

Consequently, previous low-power schottky (LS) designs like, AM26LS31 or SN75176 will in general radiate more emissions than newer Advanced Low Power designs like SN75ALS192 and SN75ALS176 or even the new BiCMOS designs like AM26C31 and SN75LBC176. A measurement was made to demonstrate this effect comparing AM26LS31 with SN75ALS192. Evidently, the negligible common mode signals resulting from switching the SN75ALS192 are significantly smaller than the clearly visible common mode current spikes produced by the AM26LS31.

SN75ALS19x Series For RS-422

The well proven SN75ALS19x series of drivers and receivers for RS-422-A represents some of the best speed versus power consumption alternatives in the industry today for reliable balanced line transmission over short as well as long distances. The series has found wide use in telecommunication as well as in computer applications.



DRIVERS	TYPE	IND. STD	REPLACING
SN75ALS192	QUAD	RS-422-A	AM26LS31
SN75ALS194	QUAD	RS-422-A	MC3487
SN75ALS191	DUAL 8-PIN	RS-422-A	UA9638

RECEIVERS	TYPE	IND. STD	REPLACING
SN75ALS193	QUAD	RS-422-A	AM26LS32A
SN75ALS195	QUAD	RS-423-A	MC3486
SN75ALS197	QUAD	V.10 V.11	AM26LS32A
SN75ALS199	QUAD	X.25 X.27	MC3486

Figure 10 - SN75ALS19x Series For RS-422

ALS Technology Advantages

Impact is a trade mark of Texas Instruments

All ALS products employ Advanced Low-Power Schottky or ImpactTM processes. These have been derived from the digital processes and trimmed for linear applications requiring wide common mode voltage operation, tough protection and accurate receiver input threshold voltages. ALS technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs - in short; speed without the usual power penalties. Standby current is typically reduced by 50% although switching speed has gone up by more than 30% compared with previous LS (Low Power Schottky) parts.

50% Lower Supply Current

The significant reduction in power consumption allows for a higher board packaging density and hence greater system integration without increasing temperature due to power dissipation. In addition, a lower operational temperature improves system reliability.
Lower power consumption also permits devices to operate in an extended temperature range (-55°C to +125°C) with fewer constraints.

30% Improvement in Data Throughput

Lower propagation delays and reduced skew, combined with lower standby power consumption, allows these devices to operate in excess of 20Mbps. For example; a SN75ALS192 quad driver is capable of transmitting data at 20Mbps (50% duty cycle) while only dissipating the same power as an AM26LS31A in standby mode. The maximum achievable data rate is usually determined by maximum power dissipation at the maximum operating temperature. Reference should be made to the data sheet's Dissipation Rating Table.

Reduced Skew

The SN75ALS19x series has been designed with minimum skew to improve symmetry, increase noise immunity and radiate less EMI (Electromagnetic Interference) caused by noncommon mode currents in the transmission cable. The high-speed dual driver, SN75ALS191 in an 8-pin package features a typical differential skew of 1.5ns (4ns maximum).

Products

A wide range of SN75ALS19x products are available as improved pin for pin replacements for industry standard devices.

The main difference between the quadruple drivers, SN75ALS192 and SN75ALS194, is related to their enabling configuration. SN75ALS192 has a common pin enabling all four drivers, whereas independent enabling schemes are possible for each pair of drivers in the SN75ALS194. Similarly, different enabling schemes distinguishes the quadruple receivers, SN75ALS193 and ALS195. The SN75ALS192 and SN75ALS193 form complementary devices as do the SN75ALS194 and SN75ALS195 devices. Using complementary drivers and receivers together should provide optimum performance.

The quadruple receivers, SN75ALS197 and ALS199 have relaxed input sensitivity specifications of ±300mV, compared to ±200mV for SN75ALS193 and ALS195. However, they are available in low cost D (surface mount) or N (DIL) packages and meets CCITT Recommendations V.10, V.11, X.26 and X.27.

AM26C31/32Low Power for RS-422

Improvements in Power Consumption and Speed

Industry has long been aware of the advantages gained from using the quadruple driver AM26LS31 and the accompanying quadruple receiver AM26LS32 for RS-422 type applications . However the old low power schottky (LS) process is no longer capable of keeping pace with today's demands for high speed and low power. The AM26C31 are AM26C32 are modern upgrades, fabricated using a low power BiCMOS process.

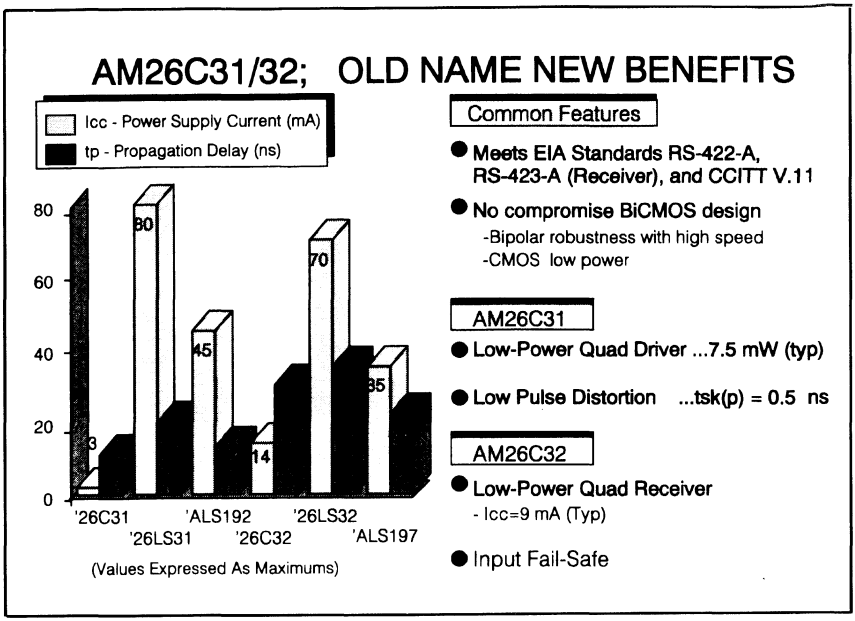


Figure 11 - AM26C31/32....Old Name New Benefits

These devices find applications where high speed and low skew are crucial, for example in disk drive and Telecommunication applications. One particular application which would benefit from the low power consumption will be the Central Office Exchange, where due to the shear number of devices used, power consumption becomes a critical issue -especially when the rest of the system is implemented in low power CMOS.

The figure shows some key benefits of these new designs and compares the power consumption and propagation delay against industry standard devices. It can easily be seen that the BiCMOS devices not only exhibit a dramatic reduction in power consumption, from 80 mA to 2 mA, but there is also an improvement in ac performance. The AM26C31 driver has a lower propagation delay than any of the devices shown in the graph.

Description

Both the AM26C31 and AM26C32 have been manufactured using a BiCMOS technology which is a combination of bipolar and CMOS transistors. This process provides the high voltage/current drive of bipolar with the low quiescent power consumption of CMOS. The graphs in the figure show that the power consumption of

the AM26C32 receiver is reduced to approximately one-fifth of the standard LS part.
The AM26C31 is a quadruple complementary-output line driver designed to satisfy the requirements of EIA RS-422-A and CCITT recommendation V.11. The three-state outputs have a high-current drive capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable input.
The AM26C32 is a quadruple line receiver for balanced and unbalanced digital data transmission. Conformance to the EIA standards RS-422-A and RS-423-A and CCITT recommendation V.11 is guaranteed. The enable function is common to all receivers and offers a choice of either active-high or active-low inputs. Three-state outputs permit connection to a digital data bus. Fail safe circuitry design on the receiver input side ensures that the outputs will remain in a high state even if the inputs are left open. This reduces the chances of incorrect data interpretation.

Hard Wired Fail Safe For RS-485

The feature of fail safe protection is also a requirement in many RS-485 applications, however its usefulness needs to be considered and understood at an application level.

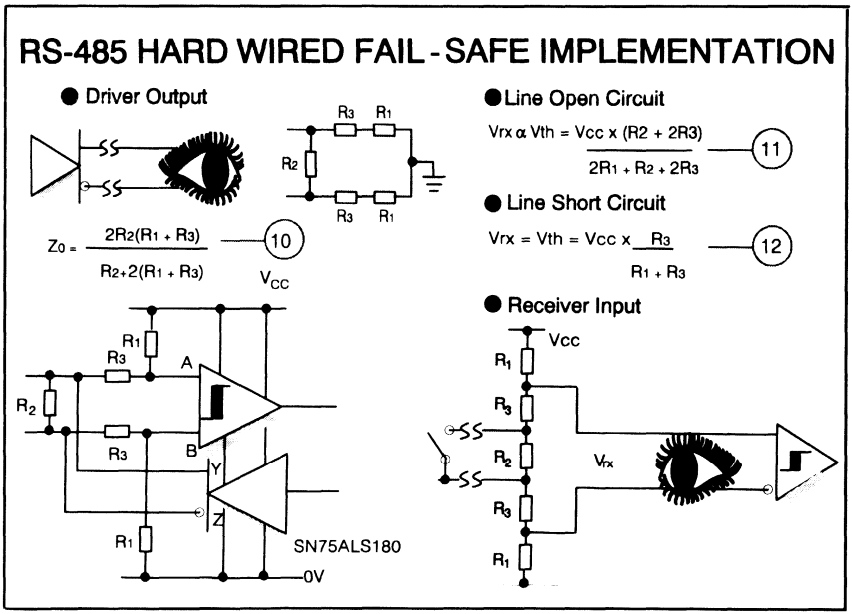


Figure 12 - RS-485 Hard Wired Fail Safe

The need For Fail Safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or a low logic state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called fail safe. An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

There are several ways implement a fail safe, including a hard-wired fail safe using line bias resistors or protocols. Protocols, although complicated to implement, are the preferred method and are discussed in more detail following this section. However since most system designers, hardware designers in this case, prefer to implement such functions in hardware a hard-wired fail safe is often implemented.

A hard wired fail safe should provide a defined voltage across the receiver's input whether or not the line is shorted to either supply rail or is left open circuited. The fail safe should also be incorporated into the line termination network when at the extremes of the line.

Internal Fail safe

Manufacturers have gone part way to facilitating fail-safe design by including some form of open line fail†safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved little use. The extra circuitry is quite often just a large pull-up resistor on the non-inverting receiver input, and a large pull-down resistor on the inverting input of the receiver. These resistors are normally in the range of 100kΩ, and so when used in conjunction with line termination resistors to form a potential divider, only a few milli volts are generated. As a result this voltage (receiver threshold voltage) is insufficient to switch the receiver. In effect, to use these internal resistors no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an ac. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedance's. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Placing external pull-up and pull-down resistors R1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic impedance, Zo , produces a potential divider between 2R1 and Zo.
The voltage formed across the line, Voc, equals

$$Voc = Vcc * \frac{Z_o}{2R_1 + Z_o}$$

Devices meeting the RS-485 receiver threshold voltage specifications require Voc to be greater than 200mV . From this the relationship of R1 to Zo can be derived:-

$$R_1 = Z_o * \frac{1}{2} * \frac{V_{cc} - V_{oc}}{V_{oc}}$$

With V_{cc} = 5V, V_{oc} = 200mV and Z_o = 100Ω, yields R_1 = 1.2kΩ.
Biasing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers it is not possible to provide shorted line fail safe configurations, this is a result of the driver and receiver sharing the same I.C. pins. Hence for devices like the SN75ALS176 this open line configuration the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the

input to the receiver can provide shorted line fail safe protection.

The extra resistors, R3 in the figure, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R3 would cause extra attenuation of the output signal. The ALS180 will have its driver outputs fed directly to the line, bypassing resistors R3.

Calculating the Resistor Values

If the line became shorted then R2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{cc} \times R_3/(R_1 + R_3) \qquad \textbf{(a)}.$$

For RS-485 and 422A applications the standard specifies Vrx to be greater than 200mV. So Vrx = Vth = 200mV. Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R1 and R3.
When the line goes into a high impedance state the receiver will see the two R3 in series with R2 plus the two R1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{cc} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \qquad \textbf{(b).}$$

Relating this new Vrx to the minimum specified in the standard, V_{th}, gives:

$$R_1 = {}^1/_2 R_2 \times [\{(V_{cc} - a\ V_{th})(V_{cc} - V_{th})\}/\{(a - 1)\ V_{th}\ V_{cc}\}]$$

$$R_3 = R_2 \times (V_{cc} - V_{th})/V_{th}$$

The transmission line will see an effective line termination resistance of R2 in parallel with twice the sum of R1 and R3. This should match the transmission line's characteristic impedance, Zo, therefore

$$Zo = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \qquad \textbf{(c)}$$

Combining equations **(a)**, **(b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = {}^1/_2 Zo \times \frac{(V_{cc} - V_{th})^2}{(a - 1) V_{th} V_{cc}}$$

$$R_2 = Zo \times \frac{V_{cc} - V_{th}}{V_{cc} - {}^aV_{th}}$$

$$R_3 = {}^1/_2 Zo \times \frac{Vcc - Vth}{a - 1 V_{th}}$$

In this application assuming the supply voltage is 4.5 V and Vth = 200 mV with an a value a of 1.5 and driving a line with characteristic impedance of 120 Ω yields the following values:-

R1 = **2.2k Ω**
R2 = **120 Ω**
R3 = **110 Ω**

The values of R1, R2, and R3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R1 and R3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers are the same, all R1 resistors are the same, and that all R3 resistors are the same. Since all of R1 and all of R3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 18k Ω.

Use of Protocols- Synchronous Serial Communication

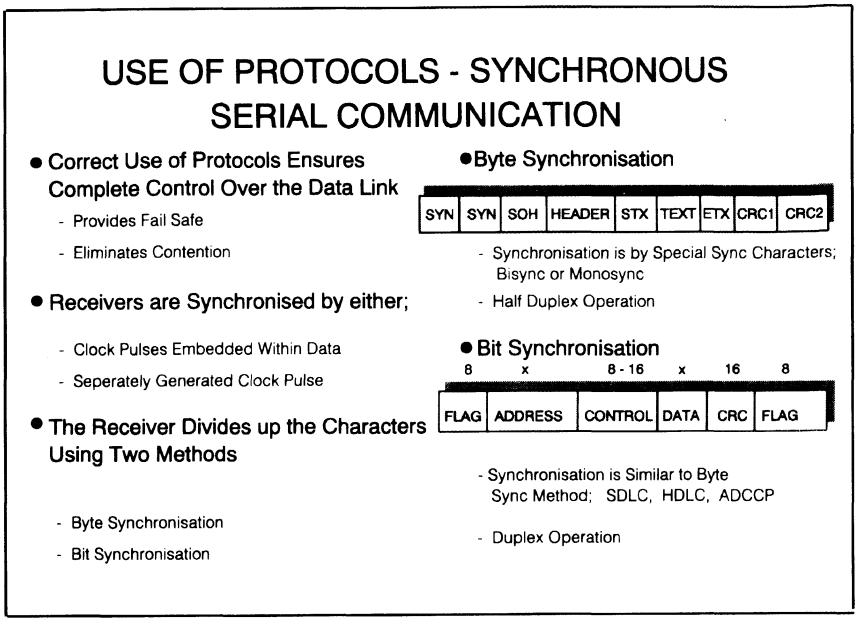


Figure 13 - Use of Protocols- Synchronous Serial Communication

The use of line terminations to effect a fail safe is not a recommended practice. The recommended practice is to use software protocols. Protocols come in many forms (two of which are explained below) and provide a set of rules which define the meaning and order in which data should be sent. In particular, they can be used to provide a fail safe feature and be used to avoid contention. Contention occurs when several drivers try to address the link at the same time. This can lead to high current sinking or souring leading to excessive thermal dissipation in the drivers. Fail safe is ensured by allowing the receiving station to respond to valid data only., This is achieved by sending a preamble before each data packet . The preamble consists of a pre-determined pattern of bits, which signals to the receiver that valid data is about to follow. Anything other than this preamble should be ignored by the receiver.

Party Line Protocol Formats

Party line applications use either half duplex or full duplex transmission. Half duplex's transmission mode is where two terminals (a driver and receiver) can communicate with each other bi-directionally over the same link, but they cannot transmit simultaneously. A party line transmission line format can be achieved using half duplex by multiplexing between a number of driver/receiver pairs. Full duplex communications involves the simultaneous, two way flow of data from driver / receiver pairs.

A communication line used in a multiplexed operation such as the half duplex party line system reduces wiring costs when compared to the simplex operation (simplex one driver for one receiver). Only one line is needed to implement the communication system, though control of the multiplexing does require complex protocol or handshaking circuits.

A typical (simplified) protocol sequence would contain the following elements;

i) **Driver requests access to communication link (bus)**
ii) **Link controller responds to request and gives go ahead when bus is free**
iii) **Driver gains bus master ship and sends data which is preceded by a destination code**
iv) **Receiver sends an acknowledgement**
v) **Driver receives confirmation and releases the bus**

Synchronisation

Some form of synchronisation is necessary for the receiver to determine the start and finish of the received bits. Two schemes, with many variations, are adopted; **Asynchronous** and **synchronous**. Asynchronisation, or start-stop bit communication, uses a system where characters are sent one at a time, without necessarily having any fixed time relationship between each other. In such a case the driver sends start bits followed by the information field, followed by one or more stop bits. This informs the receiver that information data will follow the start bit and will end prior to the stop bit. The data is usually broken into small groups of 8-bits, one byte, which is proceeded with a start bit and concluded with a stop bit. This is one of the schemes employed by EIA-232.

Synchronous transmission is used to transmit complete blocks of data at one time. In synchronous transmission the duration of each bit is the same. With all characters being the same length the receiver only has to identify the first character and then clock the others in at a predetermine rate.

Serial synchronous communication uses a similar scheme and either embeds the timing information in the data or provides a separate clock signal. However the bit stream still has to be divided up into the individual characters. There are two main methods of achieving character synchronisation: **Byte synchronisation** and **bit synchronisation.**

Byte synchronisation, one of the first synchronous methods to be introduced is best known by IBM's bisync and monosync . Synchronisation is achieved by using special SYNC characters which are transmitted in between data packets. The receiver continually monitors this transmission and uses it to synchronise itself . After receiving one (monosync) or two (bisync) sync pulses the receiver is said two be in the synchronised mode and is ready to receive data. Synchronisation is ensured by re-sending the sync bits every few hundred characters, for this reason data is grouped together in frames or packets which start with sync characters. Each frame is 8-bits long

The bisync protocol also defines a structure for a frame that includes control information and error checking capability. The figure shows the basic frame structure with the sync characters followed by the header field. SOH identifies the beginning of the header block. The header field is user defined and generally contains control specific information such as rest data link, message numbering priority ..etc. Start of text, STX, identifies the end of the header field and defines the beginning of the text field. The text or data field contains application specific information which must be sent to the application controller intact. ETX signals, end of text, and CRC1 and CRC2 are used as cyclic redundancy check bits. Notice that STX, ETX etc.. are the standard ASCII control codes. Bysync is essentially a half duplex system because each frame requires an acknowledge from the receiver before commencing with the next frame. Obviously sending acknowledging codes back and forth reduces the data rate, and to overcome this bit synchronisation was developed.

SDLC (synchronous data link control), again made popular through IBM, was one of the first bit synchronisation protocols available. The CCITT also adapted this standard for their high level data link (HDLC) protocol. Both are very similar to the CCITT X25 layer 2 packet switching local area networking standard. Initially bit sync looks very similar to byte sync , i.e. during data null periods sync pulses are sent over the link to synchronise the receiver and driver. However after the sync period the data may be grouped in any number of bits. Byte-sync systems are restricted to 8-bit packets. In SDLC and HDLC, messages are formatted into frames with each frame being divided into fields. The start flag is the sync data while the address field contains the destination address to select the required receivers. The control field can be configured as either an information field or supervisory field. The information field, which is the usual format, contains status information on the number of frames sent or received. Data field follows and contains application specific code. The supervisory or management frame is used to acknowledge successful receipt of data. CRC is used for error checking and flag is the next sync signal.

Party Line Considerations

The following points should be considered for correct party line operation;

i. Each driver must have a three-state logic capability, two logic states and a high impedance mode. Also at any one instance it is likely that all drivers could be in the high impedance state, thus leaving the bus floating. A receiver should be able to detect this situation and protect against any spurious information - fail safe design.
ii. Receivers may oscillate if left unconnected, which might affect other used receivers in the same package. Therefore it is recommended that all unused receiver inputs should be tied to defined logic states.

Input Protection In Noisy Environments

In addition to fail safe protection, applications often require protection against excessive noise voltages.

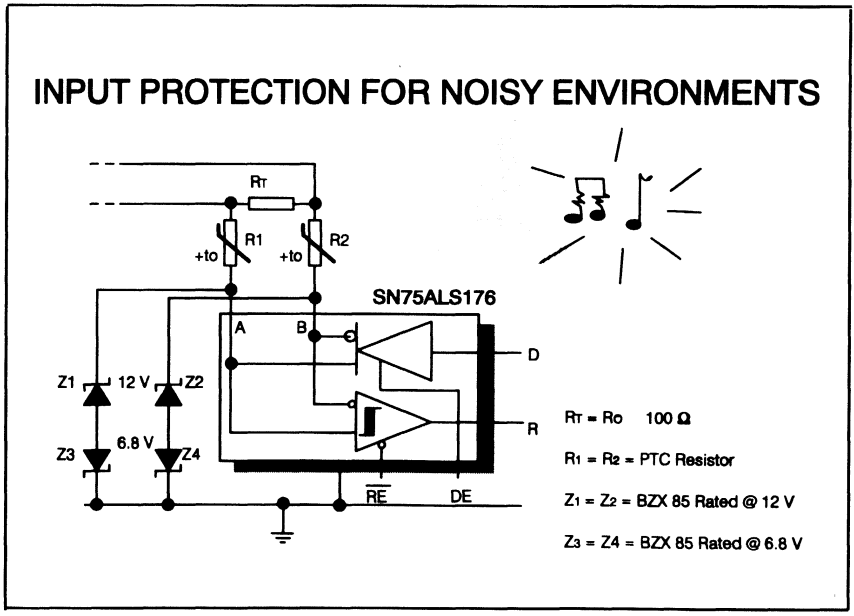


Figure 14 - Input Protection In Noisy Environments

Often when sending data over long distances or in electrically hostile environments, i.e. factory automation, the noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 is insufficient. This figure shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z1 and Z2 are chosen to protect the input from positive spikes greater than 12 V whilst Z3 and Z4 protect the device from negative going spikes greater than -6.8 V.

Calculation of Termination Resistance

The previous examples show the use of terminating resistors, the following text explains how to calculate this value..
To give better performance the transmission line needs to be terminated by a resistor of a value close to its characteristic impedance. One question that immediately arises is the value of terminating resistance required if the line is loaded by other receivers. More specifically, does the receiver's input impedance have any effect?, especially when many receivers may grouped together at the far end of the line. The following text sets out to prove that for the majority of applications the loading effect of receiver stations can be ignored and as a rule of thumb (working approximation) the value of R_T should equal the characteristic impedance of the line.

In fact, the characteristic impedance varies very little with respect to the physical dimension of the cable. For example a wire over-ground transmission line with a wire diameter equal to the diameter of an electron and a height above the ground plane of 500,000Tm (50 light years) has a characteristic impedance, Z_O, of 300Ω.

Each input of the receivers has a nominal input impedance of 18 kΩ feeding into a diode-transistor- resistor biasing network, this is equivalent to an 18 kΩ input resistor tied to a common mode voltage source of 2.4 V. -It is this configuration which provides the large common range of the receiver required for RS-485 systems.

Due to the fact that the each input is biased to 2.4V, the normal common-mode voltage of balanced RS-485 systems, the 18k W resistors on the inputs can be taken as being in series across the input of each individual receiver.
If thirty such receivers are placed close together at the end of the line, they will tend to react as thirty 36 kW resistors in parallel with the termination resistor. This overall

effective resistance will need to be close to the characteristic impedance of the line.

The effective parallel receiver resistance, R_P, will therefore be equivalent to;

$$R_p = 36 \times 10^3 / 30 = 1200\ \Omega .$$

While the termination resistor, RT, used will be equal to;

$$R_T = R_O / [1 - R_O/R_P] .$$

Thus for a line with a characteristic impedance of 100Ω, the termination resistor R_T should be:

$$R_T = 100 / [\ 1 - 100/1200] = 110\ \Omega$$

Since this calculated value is within 10% of the line characteristic impedance the value chosen for the line termination resistor, R_T, will normally be equal to the characteristic impedance, Z_O.

Methods of Connection

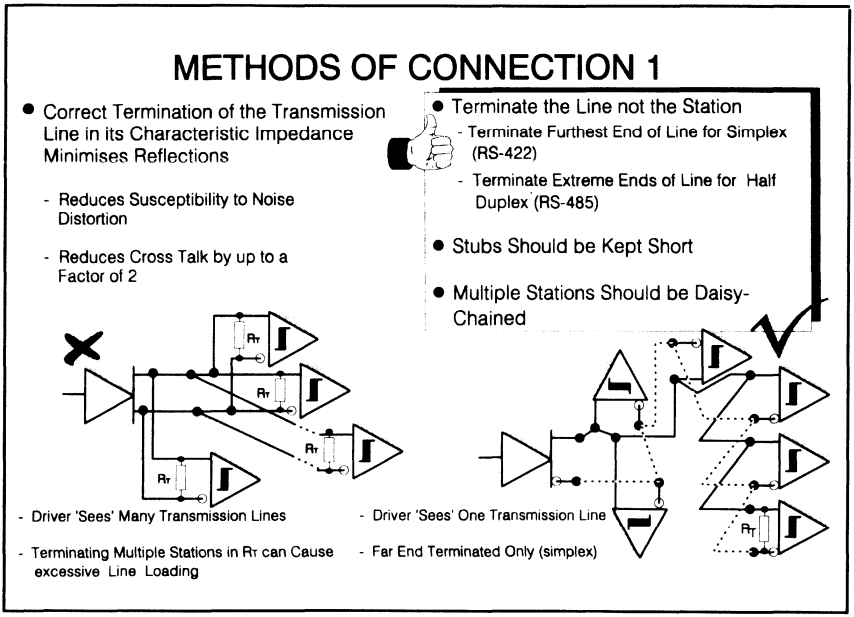


Figure 15 - Methods of Connection 1

As well as line termination the way in which stations are connected to the line needs careful consideration. Furthermore the position of the line termination resistor and device positioning must be considered. There are two basic methods of connection;

i. The star connection

ii. The daisy chain connection

Considering the star connection, the transition edge from the driver will be loaded by a group of separate transmission lines, rather than one. Each transmission line boundary will cause a change in impedance resulting in reflections.
Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.
The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and hence the driver will see one continuous transmission line with only one termination resistor. Each tap-off will in effect be a stub, but in this case they will not be all grouped together and will be kept very short to reduce their effect.

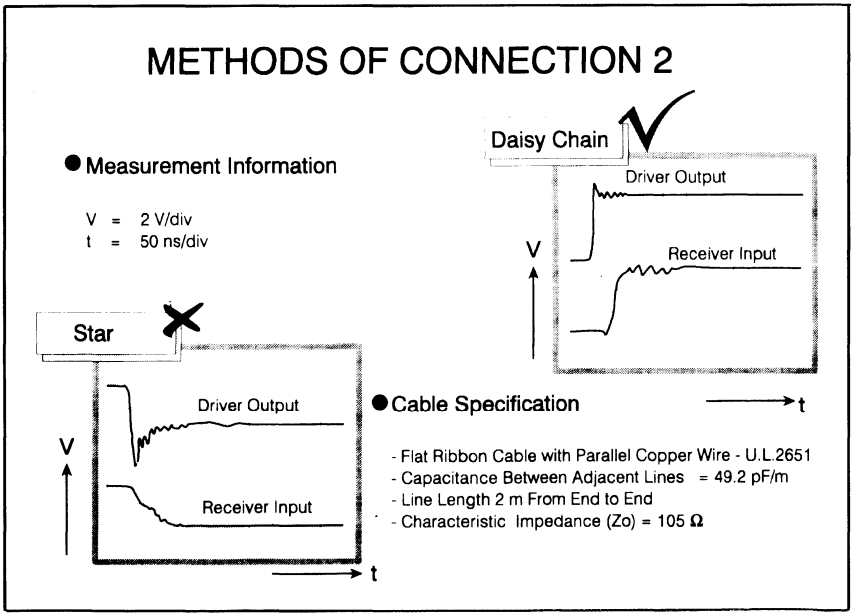


Figure 16 - Methods Of Connection 2

The figure shown further confirms the need to keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.
In both instances exactly the same application scenario was used as was the same cable specification. The cable used was a flat ribbon cable with parallel copper wire conforming to U.L. specification 2651. Connections were made as shown in the previous figure and the total cable length from source to destination was 2 m.

Calculation of Stub Length

In the earlier section a rule of thumb was developed which stated that if signal distortion is to be avoided, all connections to the main line must be kept as short as possible. Distortion in this context could be both amplitude and phase distortion - leading to reflections amongst other undesirable factors.

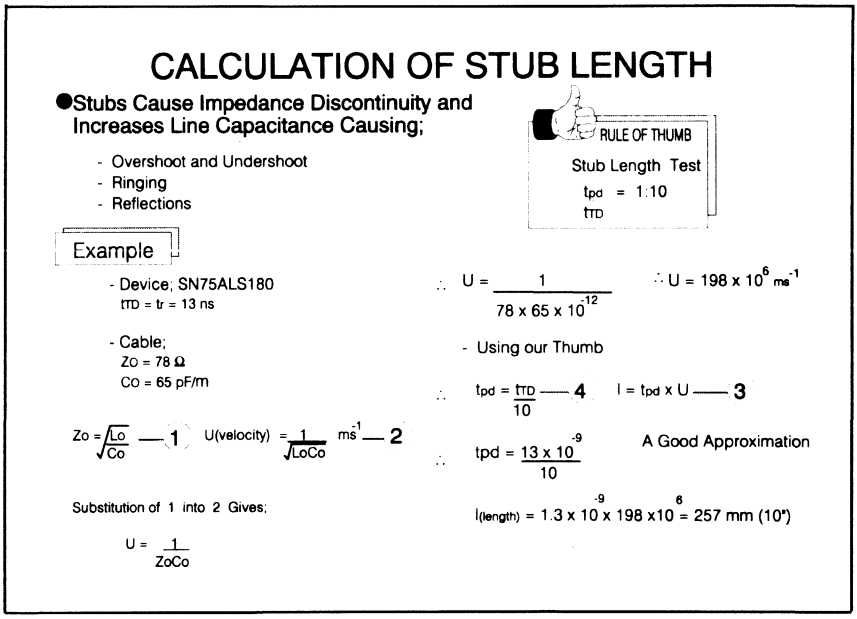


Figure 17 - Calculation of Stub Length

These connections are usually termed stubs. A stub is a connection to the transmission line from either a driver or a receiver . However, even when short in comparison to the length of the main transmission line it too could exhibit transmission line effects. Any connection to the line will cause an impedance discontinuity, leading to reflection

at the stub/transmission line boundary.
To minimise these effects the stub should be kept as short as possible, so that the stub is seen as a lumped (non transmission line) rather than a distributed (transmission line) load to the line.

How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the round trip propagation delay, tpd ,is more than 5 times the transition times of the driver, t_T. The converse is true if the line is not to operate as a transmission line but as a lumped parameter model. This forms the basis of the stub length calculation given below.
The figure shows a calculation for determining the maximum length of the stub. The rule of thumb states that the transition time of the pulse sent down the line should take ten times the time taken for the pulse to propagate to the end of the stub. As a resulting any reflections will be incorporated into the transition edge.

From this basis, the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, U, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used.

The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These facts can be brought together to give the length of the stub, ls, as;

$$l_S = t_{TD} / (10)$$

Using the SN75ALS180 and its transition time of 13ns, a cable with a characteristic impedance of 78Ω and line capacitance of 65pF, gives a maximum stub length of 254 mm or ten inches.
The main effect in this case will be a slight increase in the capacitance loading of the line.

The Unit Load Concept

One final consideration needed to implement a digital data link is the number of driver / receiver elements that can be connected to the line. This is now discussed;
The maximum number of drivers and receivers that can be placed on a single communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.
One U.L (at worst case) is defined as a load that allows 1 mA of current under a

maximum common-mode voltage stress of 12 V . The loads may consist of drivers and/or receivers but does not include the termination resistors, which may present additional loads as low as 60Ω total.

The first example shows a unit load calculation for the dual SN751178 driver/receiver which offers a unit load value of 1.1 U.L meaning 29 such devices could be connected on one line. In the second example the TL3695 transceiver is used. Since this device is internally connected as a transceiver, i.e. driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is made to the receiver input resistance, 18kΩ, giving a transceiver current of 0.6mA. This can be taken to represent 0.6 U.L. which will allow up to 47 devices to be connected to the line.

Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designers risk.

The graph in the top right corner of the figure is used to define the boundaries of the unit load, and works by superimposing the voltage and current characteristics of the load upon a reference trace. A line from - 3 V is drawn at a tangent to intercept receiver input current at the 12 V point. Similarly, a line is drawn from -7 to intercept the driver leakage current at the 5 V point. The currents indicated at - 7 V and -12 V are then compared to the currents specified by the standard. The larger of the two voltage to current ratios forms the unit load value.

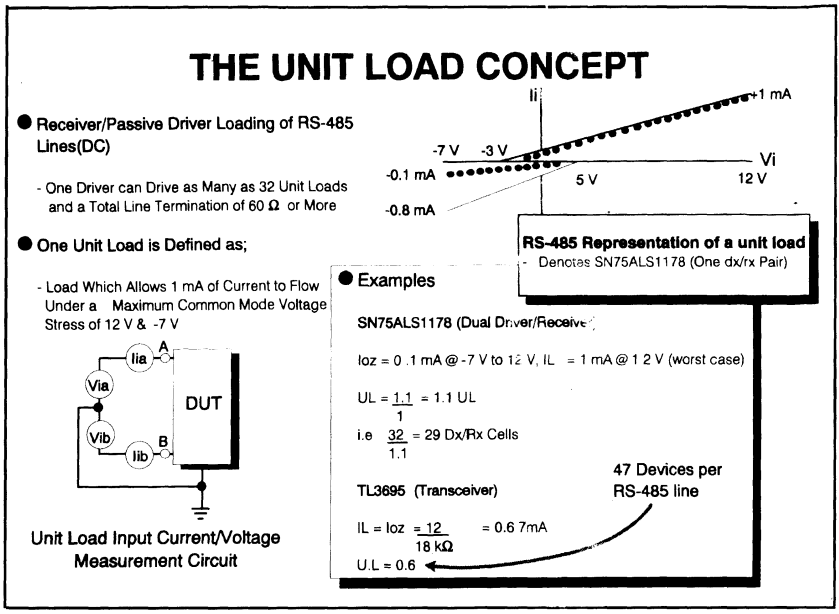


Figure 18 - The Unit Load Concept

The electrical characteristics should not show any negative resistance otherwise instability and spurious oscillations could occur.

Total Load Characteristic Limits (RS-422)

In RS-422 the dc load characteristics is specified much more simply;
The total load including multiple receivers, fail safe circuitry, and cable termination shall have a resistance greater than 90Ω between its input points (A and B), i.e. across the line, or when the cable is left un-terminated the resistance shall be greater than 400 Ω, and shall not require a differential input voltage of more than 200 mV for all receivers to assume the intended binary state.

Of the many application areas for data transmission perhaps one of the most demanding in terms of robustness is that of process automation.

Process Control Application

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application, which is shown in the figure.

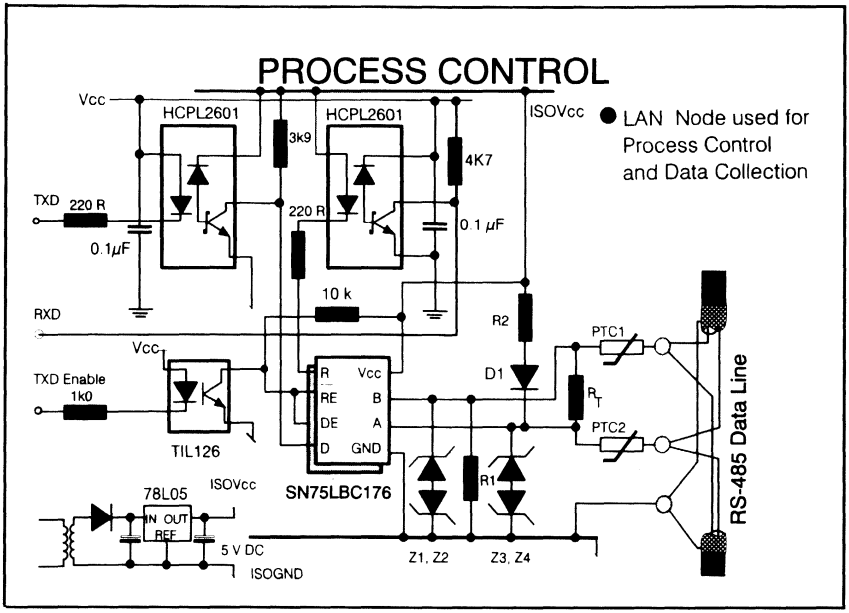


Figure 19 - Process Control Application

The need For Galvanic Isolation

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

Taking a more practical view of where problems are likely to occur when using a galvanic interface, can be found in the industrial environment. For example consider the case when the interface node, shown in the figure, connects between a data logger and a host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer

may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a 'Field bus' type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit. Other nodes, master or slaves, may be distributed along the bus in an arbitrary fashion and may be separated hundreds of metres in distance.

The bus driver used is the SN75LBC176, chosen for its low power consumption and high data rate capability. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability.

Transceiver protection circuitry is formed by Z1,Z2,Z3 and Z4 along with current limiters PTC1 and PTC2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows;

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O [1 + V_{TH}/V_{CC}]$$

Using a cable with a characteristic impedance of $Z_O = 120\ \Omega$ and a desired V_{TH} of 200 mV, requires $R_1 = R_2$ to be around 1.6 kΩ in value. The terminating resistor, R_T would be in the order of 124 Ω.

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions. The values of $R_1 = R_2$ are best kept as low as possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.
Galvanic isolation is afforded by means of three optocouplers/opto isolators. The HCPL2601 is chosen for its high data rate capability, t_p = 75 ns (max), and its high voltage isolation.
The HCPL2601 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The HCPL2601 consists of a GaAsP light emitting diode and integrated light detector, composed of a photo diode, a high gain amplifier and a Schottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of 13mA (eight 1.6mA TTL loads). A TTL input is provided for applications that require output transistor gating.

Housed in a single 8-pin dual-in-line plastic package the HCPL2601 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000V/µs.
A 0.1 µF capacitor has been connected between VCC and ground to improve switching performance.

SN75LBC176 - Ultra Low Power

The SN75LBC176 has the lowest power consumption in the industry; 1 mW vs 2.5 mW offered by the nearest low power competitor. The ac performance is also significantly better; T_{DD} of 25ns(max) vs 60 ns (max).

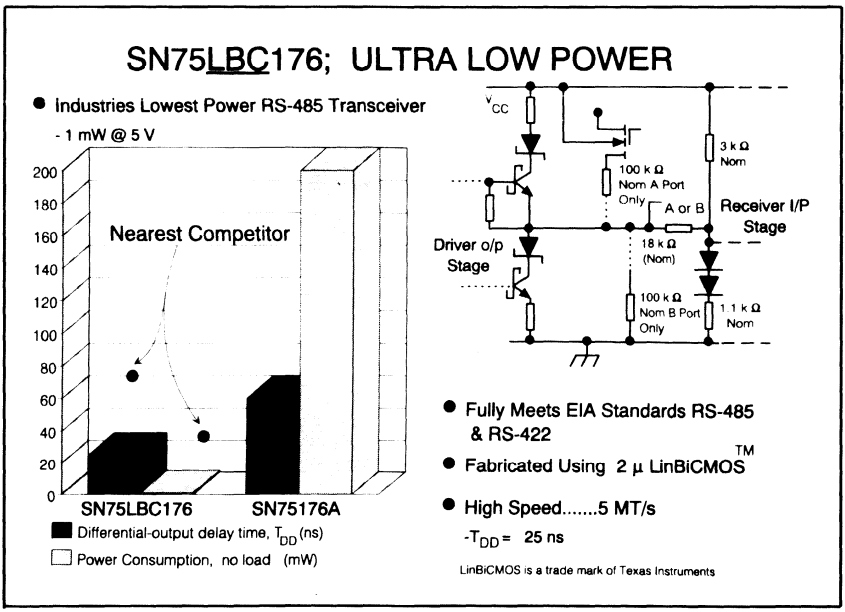


Figure 20 - SN75LBC176; Ultra Low Power

Improve MTBF

Although not representing the most glamorous end of the semiconductor design spectrum, reliable line interface circuits are crucial if the overall system mean time between failure (MTBF) is to be minimised. System designers have long been aware that often the week link in ensuing system reliability has been line interface circuits. This vulnerability is due in part to the circuits close proximity to the outside world via the edge connector. Consequently interface circuits are particularly susceptible to failure from high external voltages caused by noise, ESD or incorrect insertion of cables. For this reason the technology of choice for many Texas Instruments emerging interface products is LinBiCMOS.

LinBiCMOS, the Technology of Choice

LinBiCMOS is based on TI's highly successful LinCMOS process. LinCMOS is a 3 μm pure CMOS technology with 16 V capability, making it ideal for the design of low power analog products such as op-amps and analog-to-digital convertors (many examples of which are discussed elsewhere in this book). By shrinking the geometries to 2μm and adding a high performance 30 V bipolar structure, a new analog merged bipolar/CMOS technology has been produced.

Probably LinBiCMOS's greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost , as many "nice to have"features can make a process too expensive to address a wide range of opportunities.

By making LinBiCMOS modular, only the process modules needed to address a particular application need be used, making it very cost effective. Modules available for LinBiCMOS include high speed NPNs (with an f_T of 3GHz compared with 500MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and schottky diodes for clamping.

The Applications

With its high voltage capability and excellent switching speed LinBiCMOS is ideal to address standards such as EIA-232 and RS485. For example the RS485 standard, demands that driver output can be shorted to +12V and -7V without damage. this is particularly difficult to implement as RS485 devices are designed to operate from a single 5 V supply, meaning that parts of the chip must be designed to operate well outside its supply rails. Further more the "party line"nature of the standard requires devices that must be able to withstand contention (multiple drivers accessing the bus

simultaneous) without failure. For this reason short circuit protection and thermal shutdown are built into the chip.

The Device

The SN75LBC176 and it's extended temperature range version (-40°C to 85°C) the SN65LBC176 are high speed and low power monolithic integrated circuits designed for bidirectional data communications on multipoint bus transmission lines. Both devices fully meet the EIA (Electronics Industries Association) RS-422 and RS-485 specifications. the devices contain a single transceiver with complementary driver and receiver enable schemes and is housed in a single 8-pin package.

Using the LinBiCMOS process allows the SN75LBC176 to achieve a power supply consumption of just 1 mW (200mA at 5 V) when in the passive state. Furthermore this is achieved without the usual speed penalties; the SN75LBC176 has a driver output rise time (T_{DD}) of just 25 ns, making data rates of 5 Mbps possible.
This combination of low power and high speed is particularly relevant to todays demanding applications requiring multiple channel operation such as the small computer interface (SCSI) or telecommunication applications.

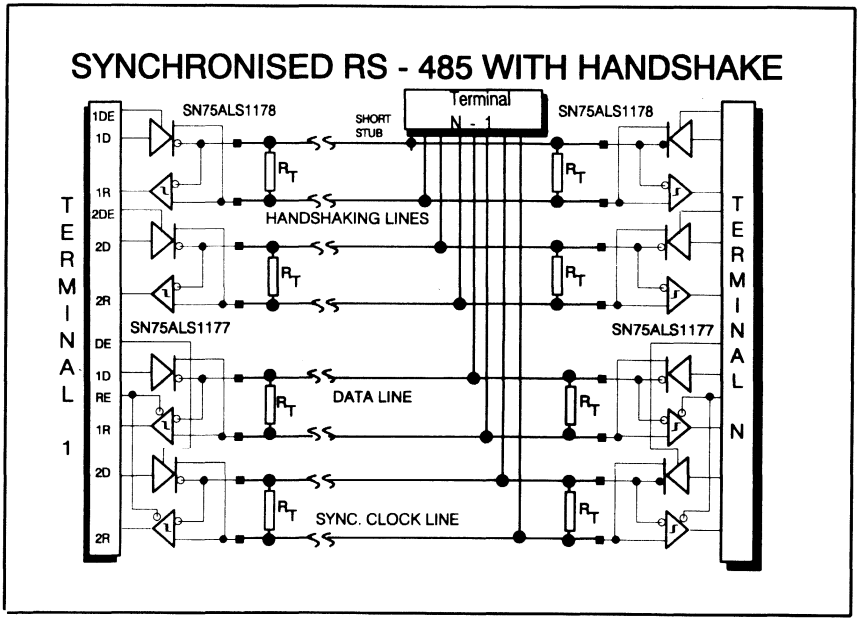


Figure 21 - Synchronised RS-485 with handshake

Synchronised RS-485 with handshake

Boost the Data Rate

Most RS-485 systems operate with a single twisted pair as the data transmission medium limiting the data transfer to asynchronous mode. In addition, the single line must also transfer receiver address, start and stop bits and a preamble to enable the receiver logic to distinguish between data or rubbish on an idle line. These additional transferred bits impact the speed of operation on the data line.

Alternatively, synchronised data transfer can be implemented by adding an additional sync. clock line as shown on the figure, and can be further complemented with the addition of a couple of handshake lines. The overall transfer of the "real data" can be significantly speeded up, as most of the control bits used in asynchronous mode will be eliminated from the data path.

Specifically, synchronous data transfer benefits from applications where complete blocks of data can be transferred because the usual requirement in asynchronous transfer for breaking the data down in small groups of 8-bits (proceeded with a start bit and concluded with a stop bit) is eliminated.

Several terminals or station can be connected to this synchronised RS-485 system. The number of stations is only limited by the usual rules for RS-485. Daisy-chain connection between terminals is required unless each terminal is connected to the main data path via a short stub as the shown for terminal number N - 1.

Why use the SN75ALS1177 and SN75ALS1178 ?

The SN75ALS1177 contains two drivers and two receivers in a single 16-pin package. Each pair of drivers and receivers has a common enable line. Upon transmission, both the data and sync. clock drivers are enabled allowing synchronous transfer of data. When shifting to receiver mode, both drivers are disabled, and the two receivers are enabled simultaneously. Due to the complementary enabling schemes for drivers and receivers (logic 1 enables the drivers but disables the receivers, and logic 0 the opposite), it is possible to connect both driver and receiver enable signals to the same control output. This reduces the number of I/O's required.

The SN75ALS1178 also contains two drivers and two receivers in a 16-pin package, but offers a different enabling pattern. The two receivers are always active and listen continuously to the handshake lines as necessary. However, the two drivers can be independently enabled as required by a handshaking scheme.

In summary, the SN75ALS1177 and SN7ALS1178 offer a simple but versatile solution

synchronous transfer of data at high speeds. Their configuration as two driver/receiver pairs adds to the effectiveness of the application

New Product Releases

1991 saw the release of several new ALS designs. Targeted towards industrial and telecommunication applications these new ALS devices offer both speed and power improvements over their existing LS counterparts. The figure shows clearly the performance advantage gained by switching to ALS designs.

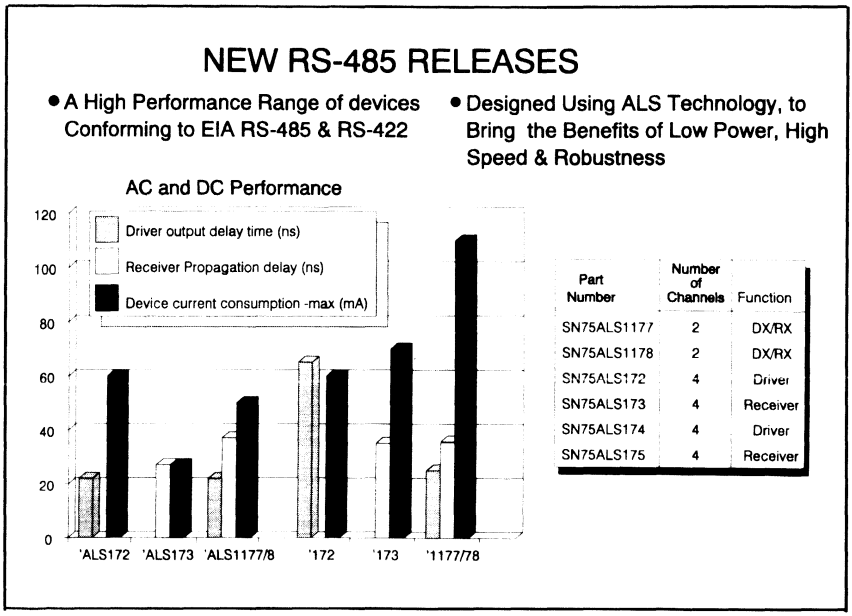


Figure 22 - New RS-485 Releases

Use of Repeaters

The major advantage of RS-485 is that it permits multiple drivers and receivers to operate over a 2-wire bus, thus setting up a party-line architecture. When such a data communication bus system is transmitting data over lines as long hundreds of meters or even thousands of metres, attenuation is often experienced between a driver at one end and a receiver in the other end (over long distances the cable's resistance does have an effect). Such systems can benefit from the use of signal restoration by means of bus

repeaters.
Similarly, when more than 32 unit loads are connected to a bus, requirements for additional buffering arise. A bus repeater has in this function a different role from restoring the original signal namely to drive another 32 unit loads.

Repeater Solutions

Bus repeaters in data communication systems receives degraded signals from the transmission line, squares up the pulses, and re-transmits the signals onto the line to the receiving station. Because the original transmitted signal is restored (squared up), the communication system becomes less susceptible to noise and other types of interference on the lines.

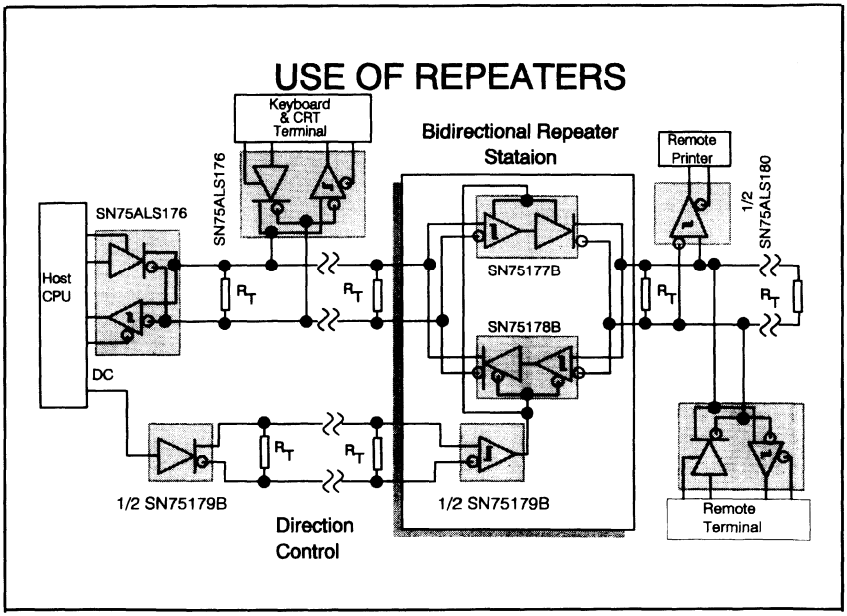


Figure 23 - Use of Repeaters

The shown "use of repeaters" application for bi-directional control of an RS-485 bus with long transmission lines is implemented with a bi-directional repeater station. Two types of repeaters are available: One version is enabled by a logic 1 control signal and the other by a logic 0. Thus, without any glue logic you can design a fully bi-directional repeater station that restores signals from both directions on a line
Enabling and disabling of the repeater drivers and receivers and thereby the data direction is controlled by the host micro-controller. In data communication systems

where no host CPU controls the data direction, intelligence needs to build into the repeater station to maintain system control. This allows also for independent communication on each side of the repeater station providing additional flexibility and faster overall data exchange.

Recommended Products

Dedicated products designed specifically for repeater purposes are the SN75177B and SN75178B. Employing these repeater devices in simple repeater stations as the shown, completely eliminates the need for any glue logic due to their enabling scheme.

Section 3

Data Sheets

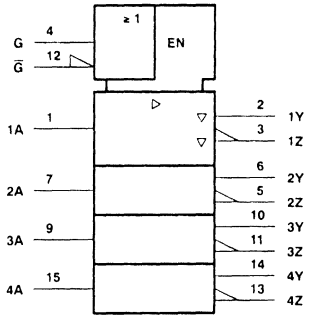
- Meets EIA Standard RS-422-A and CCITT Recommendation V.11
- Low Power, I_{CC} = 100 μA Typ
- Operates From a Single 5-V Supply
- High Speed, $t_{PLH} = t_{PHL}$ = 7 ns Typ
- Low Pulse Distortion ($t_{sk(p)}$ = 0.5 ns Typ)
- High Output Impedance in Power-Off Conditions
- Improved Replacement for AM26LS31

description

The AM26C31C and AM26C31I are quadruple complementary-output line drivers designed to meet the requirements of EIA Standard RS-422-A and CCITT V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

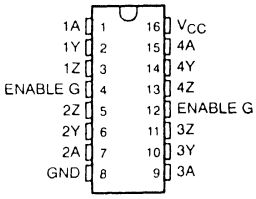
The AM26C31C is characterized for operation from 0°C to 70°C and the AM26C31I is characterized for operation from – 40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D OR N PACKAGE
(TOP VIEW)

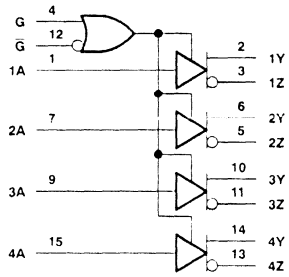


FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... – 0.5 V to 7 V
Input voltage range, V_I ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... – 0.5 V to 7 V
Clamp diode current, I_{IK} or I_{OK} ..... ± 20 mA
Output current, I_O ..... ± 150 mA
V_{CC} current ..... 200 mA
GND current ..... – 200 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: AM26C31C ..... 0°C to 70°C
AM26C31I ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				– 20	mA
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	AM26C31C	0		70	°C
	AM26C31I	– 40		85	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −20 mA		2.4	3.4		V
V_{OL}	Low-level output voltage	I_O = 20 mA			0.2	0.4	V
$\lvert V_{OD} \rvert$	Differential output voltage	R_L = 100 Ω		2	3.1		V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage‡	R_L = 100 Ω				±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω				3	V
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage‡	R_L = 100 Ω				±0.4	V
I_I	Input current	V_I at V_{CC}, V_{IH}, V_{IL}, or GND				±1	µA
$I_{O(off)}$	Driver output current with power off	V_{CC} = 0,	V_O = 6 V			100	µA
		V_{CC} = 0,	V_O = −0.25 V			−100	
I_{OS}	Driver output short-circuit current	V_O = 0		−30		−150	mA
I_{OZ}	Off-state (high-impedance state) output current	V_O = 2.5 V				20	µA
		V_O = 0.5 V				−20	µA
I_{CC}	Quiescent supply current	I_O = 0,	V_I = 0 or 5 V			100	µA
		I_O = 0, See Note 2	V_I = 2.4 or 0.5 V,		1.5	3.0	mA
C_i	Input capacitance				6		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 2: Measured per input. All other inputs are at 0 or 5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 1 and 2,	S1 is open		7	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output				7	12	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)				0.5	4	ns
t_{rD}, t_{fD}	Differential output rise and fall times	See Figures 1 and 4,	S1 is open		5	10	ns
t_{PZH}	Output enable time to high level	See Figures 1 and 3,	S1 is closed		10	19	ns
t_{PZL}	Output enable time to low level				10	19	ns
t_{PHZ}	Output disable time from high level				7	16	ns
t_{PLZ}	Output disable time from low level				7	16	ns
C_{pd}	Power dissipation capacitance (see Note 3)	No load,	T_A = 25°C		100		pF

NOTE 3: C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} V_{CC}^2 f$ where P_D is in watts, C_{pd} is in farads, V_{CC} is in volts, and f is in hertz.

PARAMETER MEASUREMENT INFORMATION

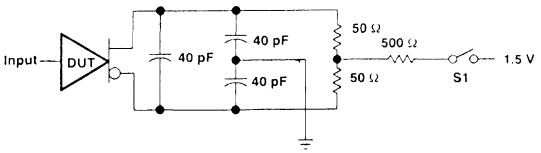


Figure 1. Test Circuit

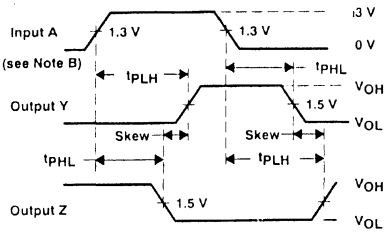


Figure 2. Propagation Delay Times and Skew Waveforms

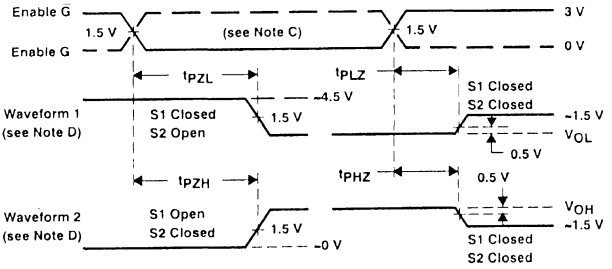


Figure 3. Enable and Disable Time Waveforms

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.
B. When measuring propagation delay times and skew, switch S1 is open.
C. Each enable is tested separately.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PARAMETER MEASUREMENT INFORMATION

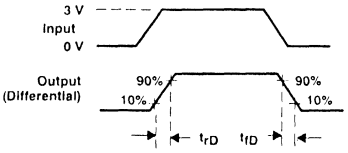


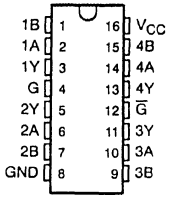
Figure 4. Differential Rise and Fall Times

AM26C32C, AM26C32I
QUADRUPLE DIFFERENTIAL RECEIVERS

JANUARY 1992

- Meets EIA Standards RS-422-A, RS-423-A, and CCITT Recommendation V.11
- Low Power, I_{CC} = 9 mA Typ
- ±7-V Common-Mode Range With ±200-mV Sensitivity
- Input Hysteresis . . . 60 mV Typical
- t_{pd} = 19 ns (Typ)
- Operates From a Single 5-V Supply
- 3-State Outputs
- Input Fail-Safe Circuitry
- Improved Replacement for AM26LS32

D OR N PACKAGE
(TOP VIEW)



description

The AM26C32C and AM26C32I are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

The AM26C32 is manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high-voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32 while still maintaining ac and dc performance.

The AM26C32C is characterized for operation from 0°C to 70°C and the AM26C32I is characterized from −40°C to 85°C.

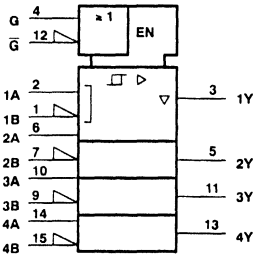
FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES G	ENABLES $\overline{G}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TH}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

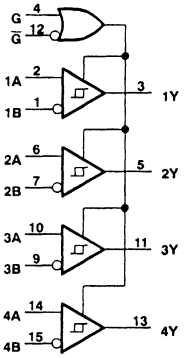
TEXAS INSTRUMENTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I: A or B inputs ..... -11V to +14V
G or $\overline{G}$ inputs ..... 7 V
Output voltage, V_O ..... 7 V
Output current, I_O ..... ±25 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: AM26C32C ..... 0°C to 70°C
AM26C32I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal. Currents into the device are positive and currents out of the device are negative.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode input voltage, V_{IC}				±7	V
High-level output current, I_{OH}				−6	mA
Low-level output current, I_{OL}				6	mA
Operating free-air temperature, T_A	AM26C32C	0		70	°C
	AM26C32I	−40		85	

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

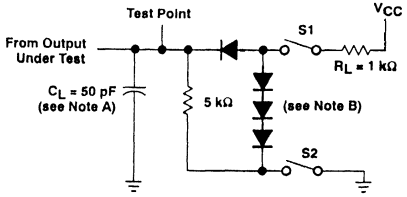
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high-threshold voltage	$V_O = V_{OH}$ min,	$I_{OH} = -440\ \mu A$			0.2	V
V_{TL}	Differential input low-threshold voltage	$V_O = 0.45$ V,	$I_{OL} = 8$ mA	−0.2‡			V
V_{hys}	Hysteresis, $V_{T+} - V_{T-}$				60		mV
V_{IK}	Enable input clamp voltage	V_{CC} = MIN,	$I_I = -18$ mA			−1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV,	$I_{OH} = -6$ mA	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV,	$I_{OL} = 6$ mA		0.2	0.3	V
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{CC}$ or GND			±0.5	±5	μA
I_I	Line input current	$V_I = 10$ V,	Other input at 0 V			1.5	mA
		$V_I = -10$ V,	Other input at 0 V			−2.5	
I_{IH}	High-level enable current	$V_I = 2.7$ V				20	μA
I_{IL}	Low-level enable current	$V_I = 0.4$ V				−100	μA
r_i	Input resistance	One input to ac ground			17		kΩ
I_{CC}	Supply current	V_{CC} = MAX	All outputs disabled		9	14	mA
			All outputs enabled		12		

switching characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

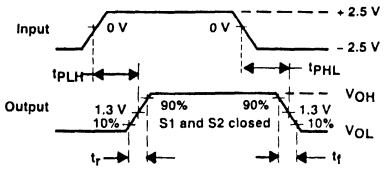
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 1	10	19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	19	30	ns
t_f	Output fall time	See Figure 1		4	9	ns
t_r	Output rise time			4	9	ns
t_{PZH}	Output enable time to high level	See Figure 1		13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level	See Figure 1		13	22	ns
t_{PLZ}	Output disable time from low level			13	22	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$, and $V_{IC} = 0$.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

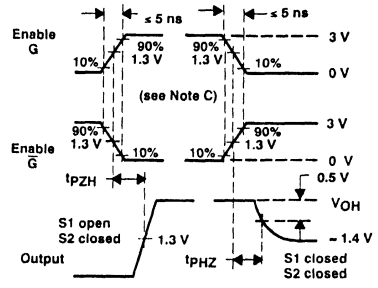
PARAMETER MEASUREMENT INFORMATION



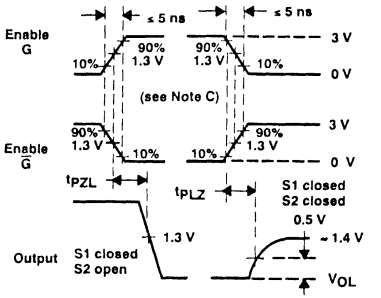
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

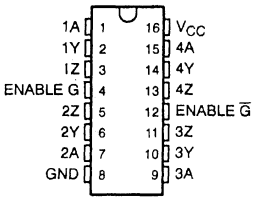
Figure 1

AM26LS31C
QUADRUPLE LINE DRIVER

MAY 1990

- **Meets EIA Standard RS-422-A**
- **Operates From a Single 5-V Supply**
- **TTL Compatible**
- **Complementary Outputs**
- **High Output Impedance in Power-Off Conditions**
- **Complementary Output Enable Inputs**

D, J, OR N PACKAGE
(TOP VIEW)



description

The AM26LS31C is a quadruple complementary-output line driver designed to meet the requirements of EIA Standard RS-422-A and Federal Standard 1020. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

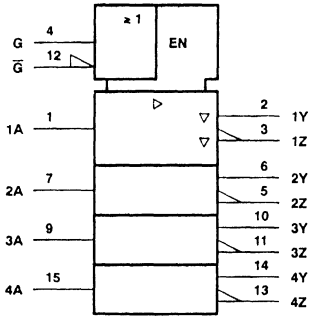
The AM26LS31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

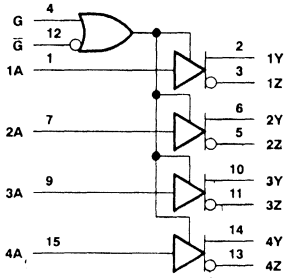
logic symbol†



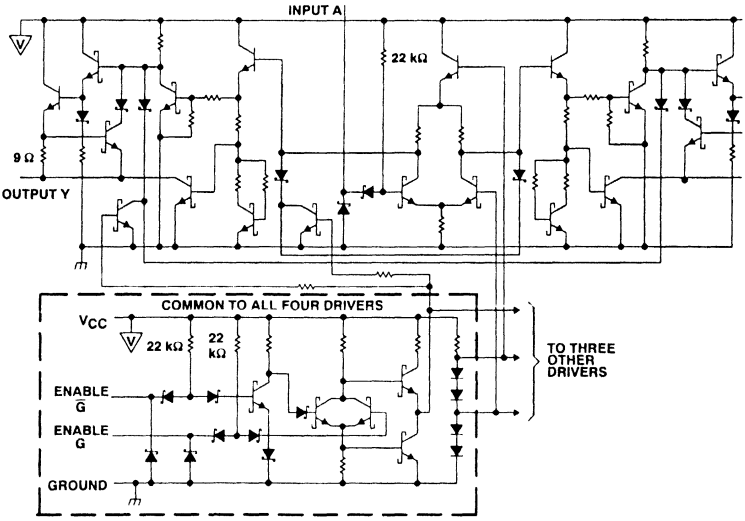
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 7 V
Output off-state voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0 to 70°C
Storage temperature range ..... – 65 to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOP ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

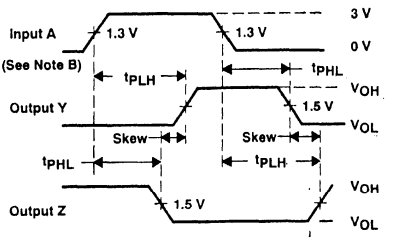
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = – 18 mA			– 1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = – 20 mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 20 mA			0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = 4.75 V	V_O = 0.5 V			– 20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			– 0.36	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.25 V		– 30		– 150	mA
I_{CC}	Supply current	V_{CC} = 5.25 V,	All output disabled		32	80	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

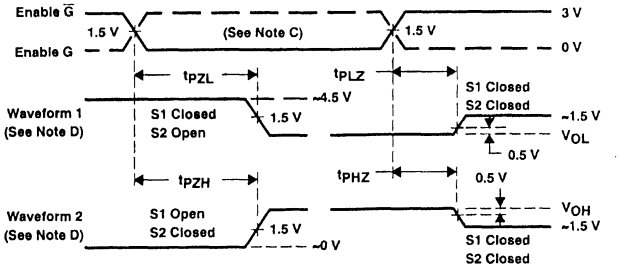
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	See Figure 1,	S1 and S2 open		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	ns
	Output-to-output skew					1	6	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF,	R_L = 75 Ω,	See Figure 1		25	40	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF,	R_L = 180 Ω,	See Figure 1		37	45	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF,	See Figure 1,	S1 and S2 closed		21	30	ns
t_{PLZ}	Output disable time from low level					23	35	ns

PARAMETER MEASUREMENT INFORMATION

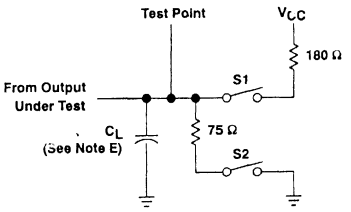


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.
B. When measuring propagation delay times and skew, switches S1 and S2 are open.
C. Each enable is tested separately.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. C_L includes probe and jig capacitance.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

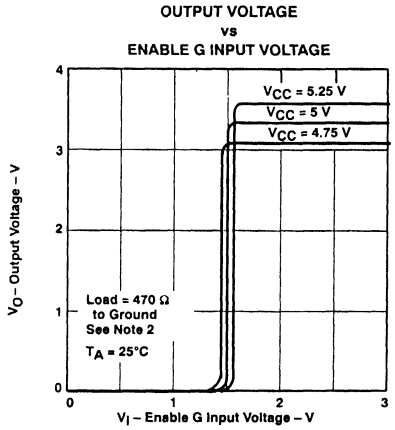


Figure 2

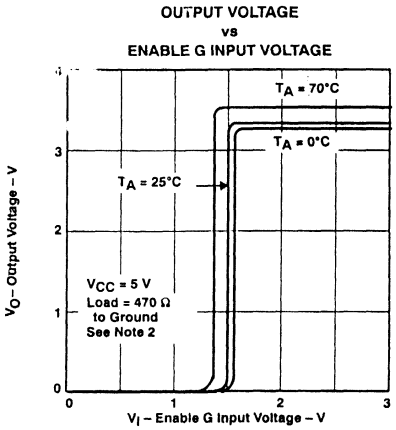


Figure 3

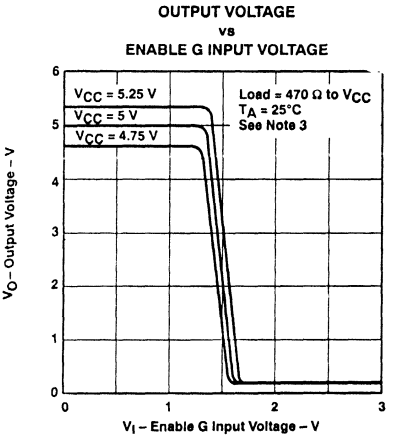


Figure 4

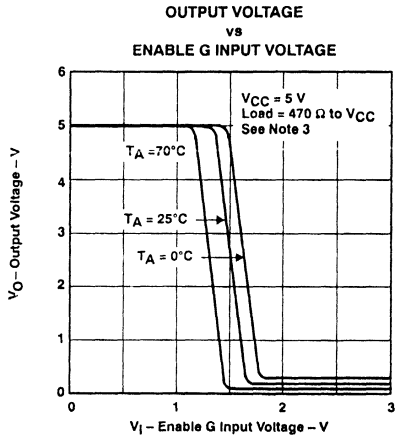


Figure 5

NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
3. The A input is connected to ground during the testing of the Y ouputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

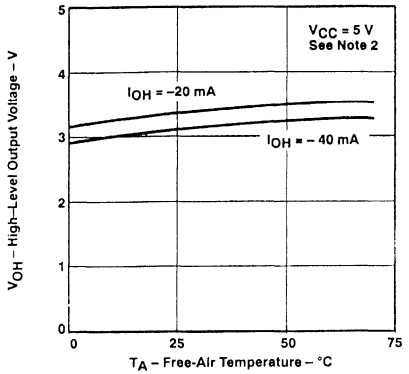


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

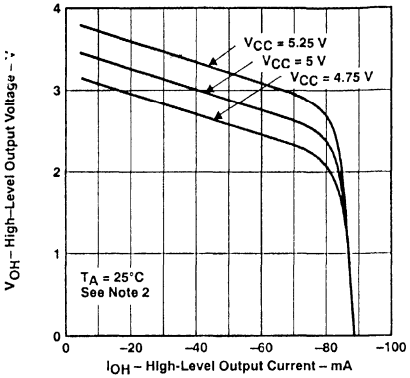


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

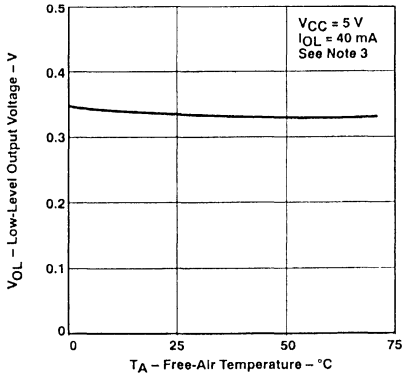


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

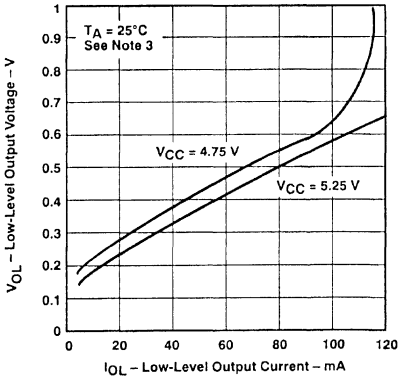


Figure 9

NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
3. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

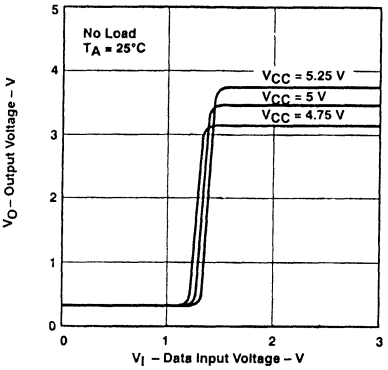


Figure 10

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

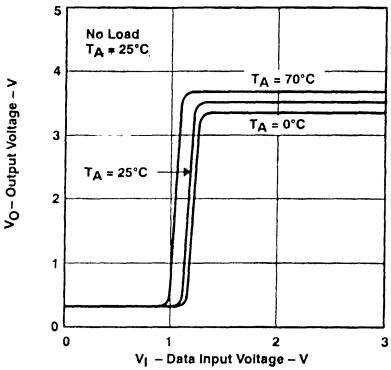


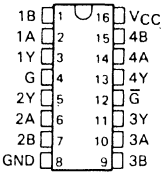
Figure 11

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

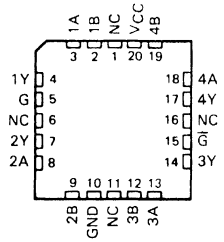
SEPTEMBER 1986

- **AM26LS32A Meets EIA Standards RS-422-A and RS-423-A**
- **AM26LS32A Has ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS33A Has ±15-V Common-Mode Range With ±500 mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32C and AM26LS33C**

AM26LS32AC, AM26LS33AC . . . D, J, OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The AM26LS32A and AM26LS33A are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

Compared to the AM26LS32C and the AM26LS33C, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and the AM26LS33AM are characterized for operation over the full military temperature range of −55°C to 125°C.

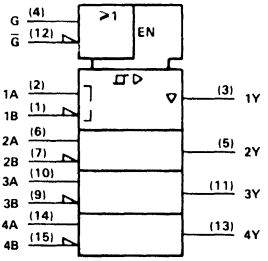
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES G	ENABLES $\overline{G}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

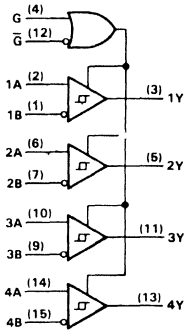
TEXAS INSTRUMENTS

logic symbol†

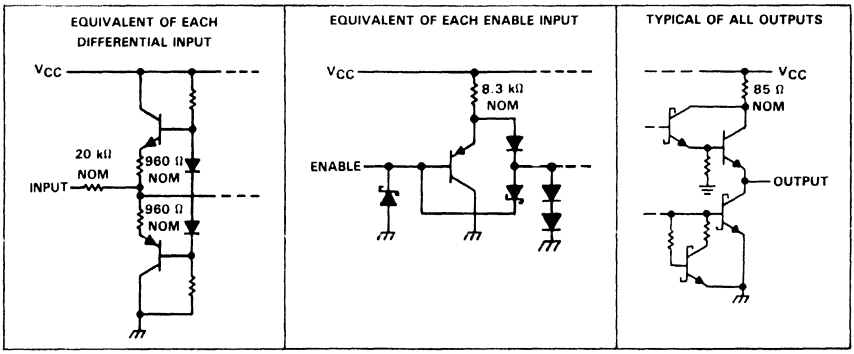


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		AM26LS32AC AM26LS33AC	AM26LS32AM AM26LS33AM	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, any differential input		±25	±25	V
Differential input voltage (see Note 2)		±25	±25	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (C-SUFFIX)	1025 mW	8.2 mW/°C	656 mW	—
J (M-SUFFIX)	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		AM26LS32AC AM26LS33AC			AM26LS32AM AM26LS33AM			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM			±7			±7	V
	AM26LS33AC, AM26LS33AM			±15			±15	
High-level output current, I_{OH}				−440			−440	μA
Low-level output current, I_{OL}				8			8	mA
Operating free-air temperature, T_A		0		70	−55		125	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

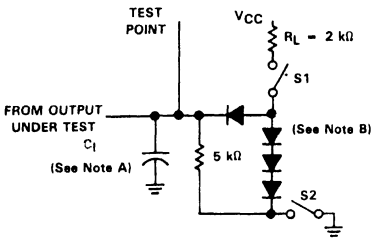
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high-threshold voltage	$V_O = V_{OH}$min, $I_{OH} = -440\ \mu A$		AM26LS32A			0.2	V
				AM26LS33A			0.5	
V_{TL}	Differential input low-threshold voltage	$V_O = 0.45$ V, $I_{OL} = 8$ mA		AM26LS32A	-0.2‡			V
				AM26LS33A	-0.5‡			
V_{hys}	Hysteresis, $V_{T+} - V_{T-}$§					50		mV
V_{IK}	Enable input clamp voltage	V_{CC} = MIN, $I_I = -18$ mA					-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{ID} = 1 V, $V_{I(\overline{G})}$ = 0.8 V, $I_{OH} = -440\ \mu A$		'32AC, '33AC	2.7			V
				'32AM, '33AM	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, $V_{ID} = -1$ V, $V_{I(\overline{G})}$ = 0.8 V		I_{OL} = 4 mA			0.4	V
				I_{OL} = 8 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX		V_O = 2.4 V			20	μA
				V_O = 0.4 V			-20	
I_I	Line input current	V_I = 15 V,	Other input at -10 V to 15 V				1.2	mA
		$V_I = -15$ V,	Other input at -15 V to 10 V				-1.7	
$I_{I(EN)}$	Enable input current	V_I = 5.5 V					100	μA
I_{IH}	High-level enable current	V_I = 2.7 V					20	μA
I_{IL}	Low-level enable current	V_I = 0.4 V					-0.36	mA
r_i	Input resistance	$V_{IC} = -15$ V to 15 V, One input to AC ground			12	15		kΩ
I_{OS}	Short-circuit output current¶	V_{CC} = MAX			-15		-85	mA
I_{CC}	Supply current	V_{CC} = MAX,	All outputs disabled			52	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
‡The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figures 10 and 11.
¶Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

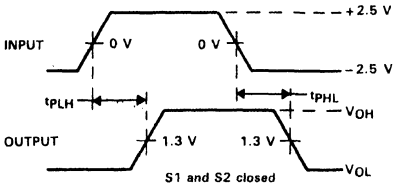
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level			20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level			30	40	ns

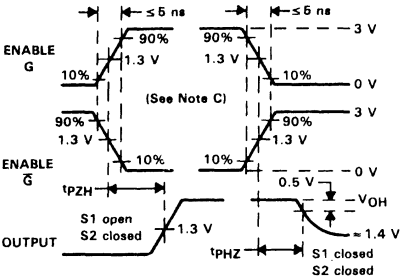
PARAMETER MEASUREMENT INFORMATION



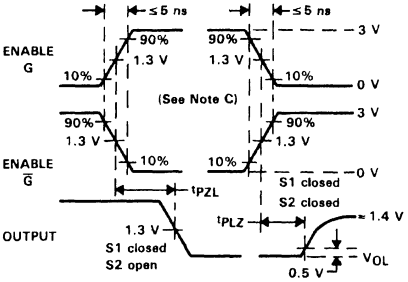
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 1

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

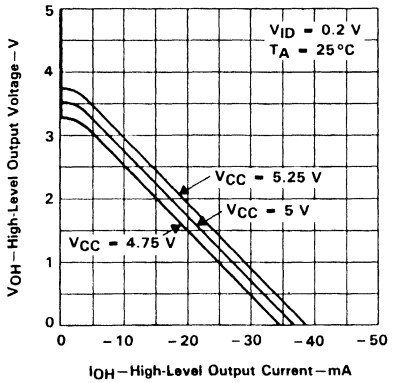


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

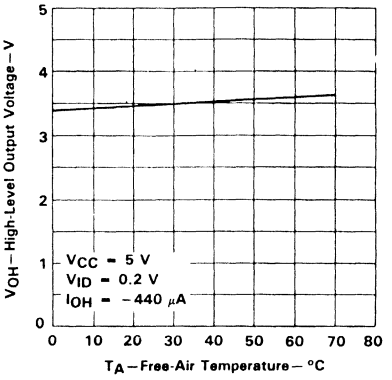


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

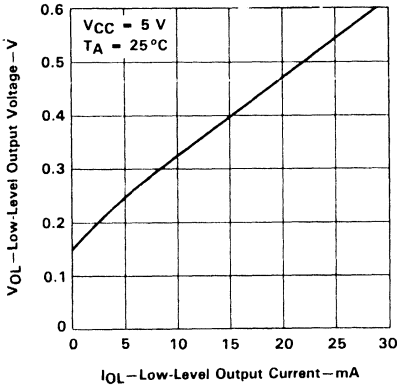


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

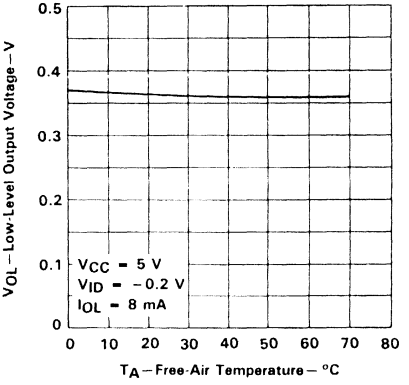


FIGURE 5

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

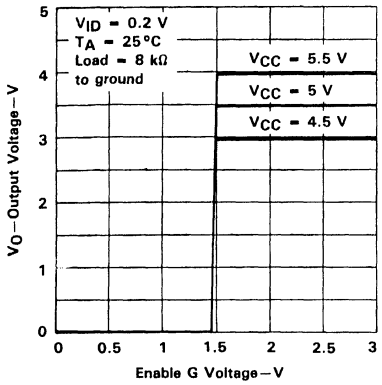


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

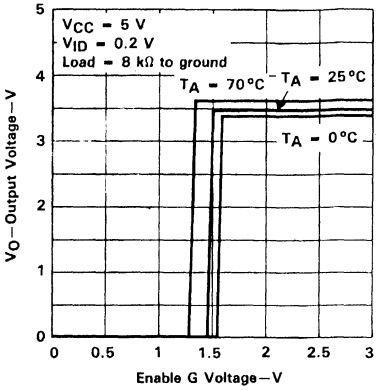


FIGURE 7

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

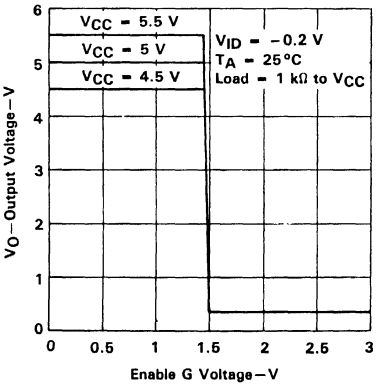


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

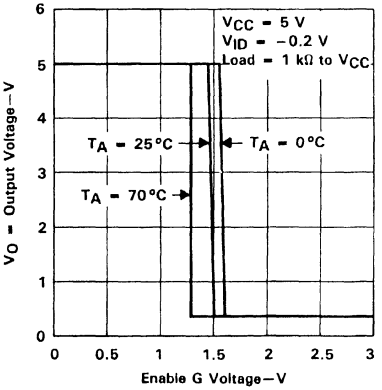


FIGURE 9

TYPICAL CHARACTERISTICS

AM26LS32A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

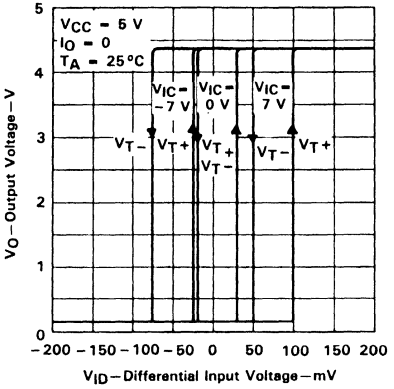


FIGURE 10

AM26LS33A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

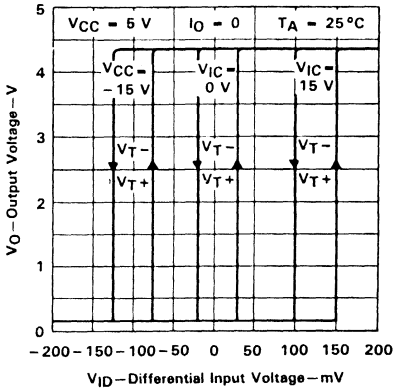


FIGURE 11

INPUT CURRENT
vs
INPUT VOLTAGE

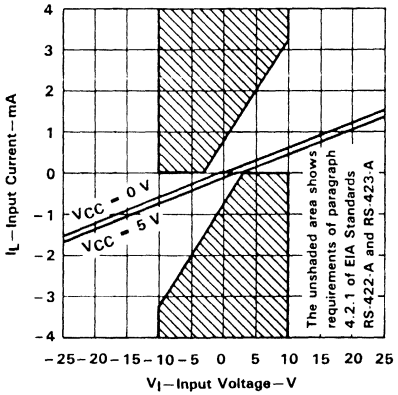
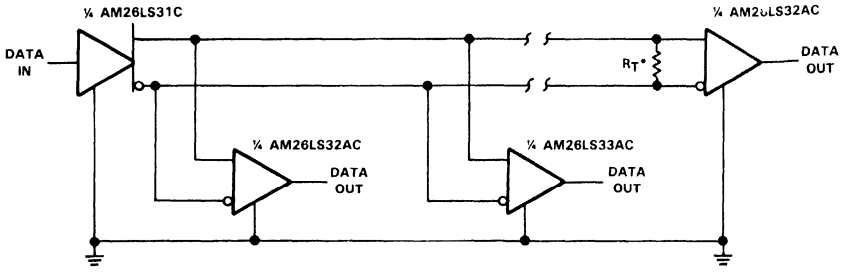


FIGURE 12

APPLICATION INFORMATION



*R_T equals the characteristic impedance of the line.

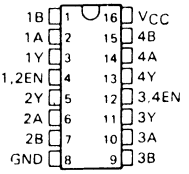
FIGURE 13. CIRCUIT WITH MULTIPLE RECEIVERS

QUADRUPLE LINE RECEIVER WITH 3-STATE OUTPUT

SEPTEMBER 1986

- **Meets EIA Standards RS-422-A and RS423-A and Federal Standards 1020 and 1030**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **Operates from Single 5-V Supply**
- **Designed to be Interchangeable with Motorola MC3486**

D, J OR N PACKAGE
(TOP VIEW)



description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of EIA Standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

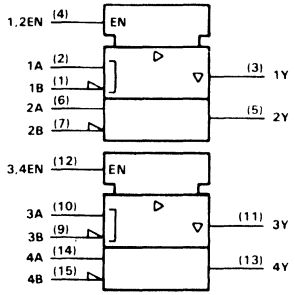
The MC3486 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} <$ 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z

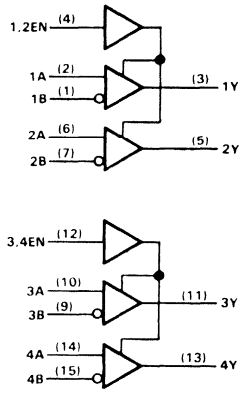
H = high level, L = low level, Z = high-impedance (off), ? = indeterminate

logic symbol†

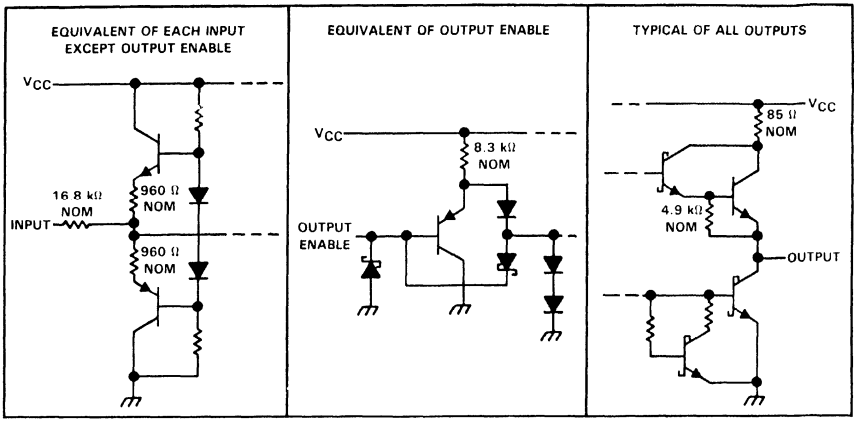


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 8 V
Low-level output current . . . . . 50 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±6	V
High-level enable input voltage, V_{IH}	2			V
Low-level enable input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2[†]		V
V_{IK}	Enable-input clamp voltage	I_I = −10 mA			−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 0.4 V, I_O = −0.4 mA, See Note 3 and Figure 1		2.7		V
V_{OL}	Low-level output voltage	V_{ID} = −0.4 V, I_O = 8 mA, See Note 3 and Figure 1			0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = −3 V, V_O = 2.7 V			40	μA
		V_{IL} = 0.8 V, V_{ID} = 3 V, V_O = 0.5 V			−40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 5.25 V, Other inputs at 0 V	V_I = −10 V		−3.25	mA
			V_I = −3 V		−1.5	
			V_I = 3 V		1.5	
			V_I = 10 V		3.25	
I_{IH}	High-level enable input current	V_I = 5.25 V			100	μA
		V_I = 2.7 V			20	
I_{IL}	Low-level enable input current	V_I = 0.5 V			−100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 V, V_O = 0, See Note 4		−15	−100	mA
I_{CC}	Supply current	V_{IL} = 0			85	mA

[†] The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 3. Refer to EIA Standards RS-422-A and RS-423-A for exact conditions.
4. Only one output at a time should be shorted.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, See Figure 2		28	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			27	30	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

PARAMETER MEASUREMENT INFORMATION

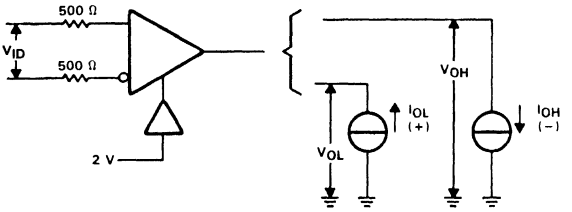


FIGURE 1. V_{OH}, V_{OL}

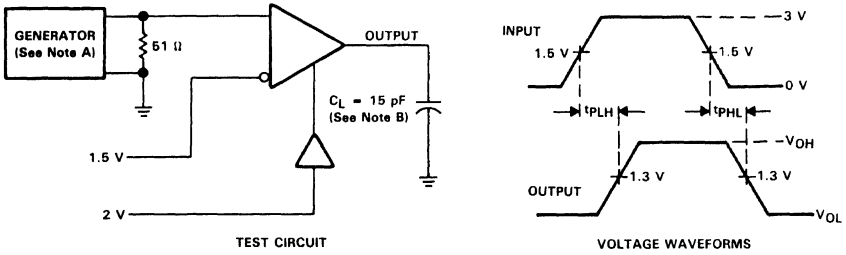
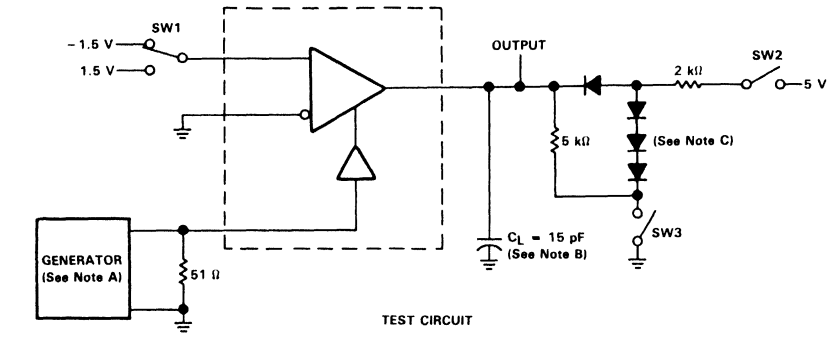


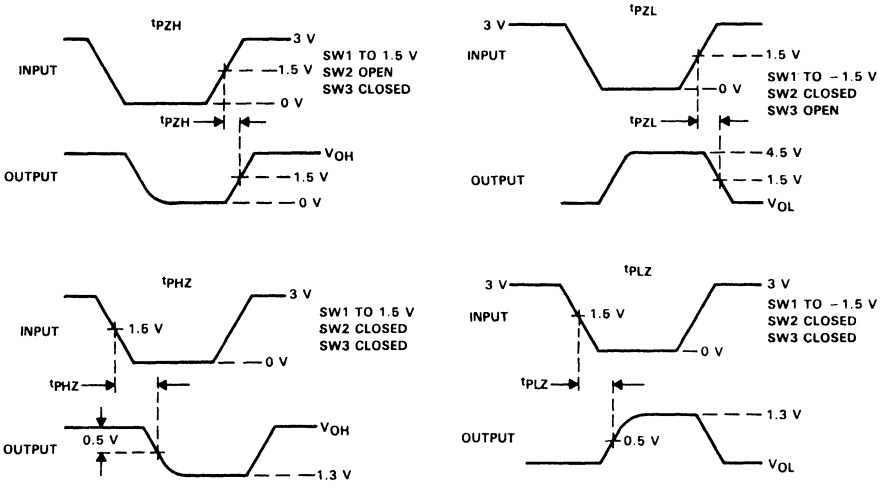
FIGURE 2. PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. ENABLE AND DISABLE TIMES

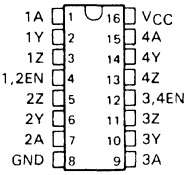
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

MC3487
QUADRUPLE DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

SEPTEMBER 1986

- **Meets EIA Standard RS-422-A and Federal Standard 1020**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**
- **Designed to Be Interchangeable with Motorola MC3487**

D, J, OR N PACKAGE
(TOP VIEW)



description

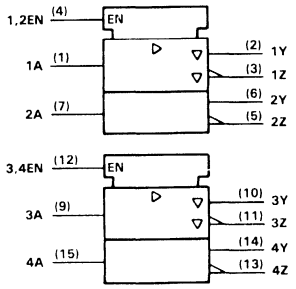
The MC3487 offers four independent differential line drivers designed to meet the specifications of EIA Standard RS-422-A and Federal Standard 1020. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low. The outputs are capable of source or sink currents of 48 mA.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

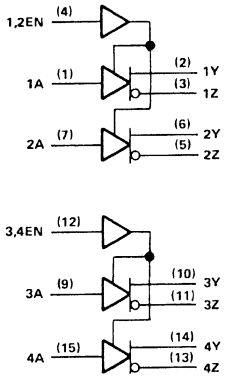
The MC3487 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



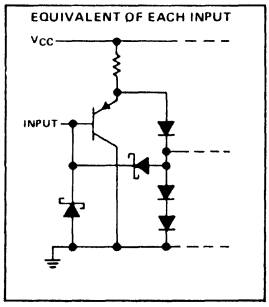
TEXAS INSTRUMENTS

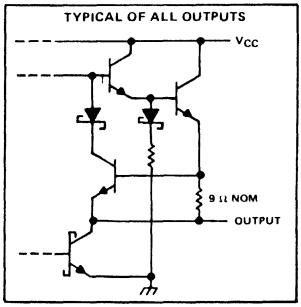
FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

H = TTL high level X = irrelevant
L = TTL low level

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = −20 mA	2.5		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\lvert V_{OD}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1		2		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	R_L = 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−400	μA
I_{OS}	Short-circuit output current§	V_I = 2 V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

†$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
‡In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
§Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	ns
	Skew			6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 4		30	ns
t_{PZL}	Output enable time to low level			30	ns
t_{PHZ}	Output disable time from high level			25	ns
t_{PLZ}	Output disable time from low level			30	ns

PARAMETER MEASUREMENT INFORMATION

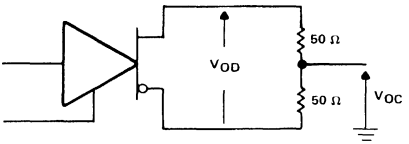


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

PARAMETER MEASUREMENT INFORMATION

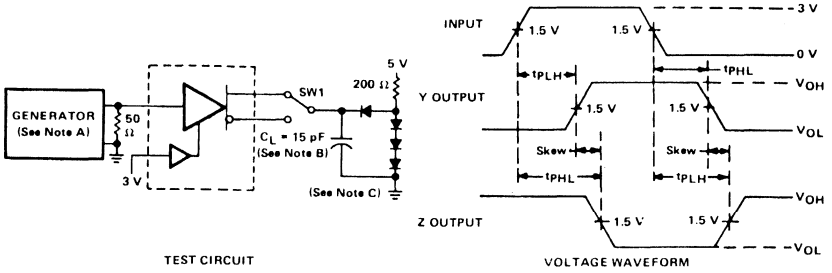


FIGURE 2. PROPAGATION DELAY TIMES

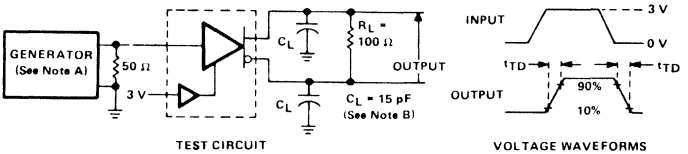


FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

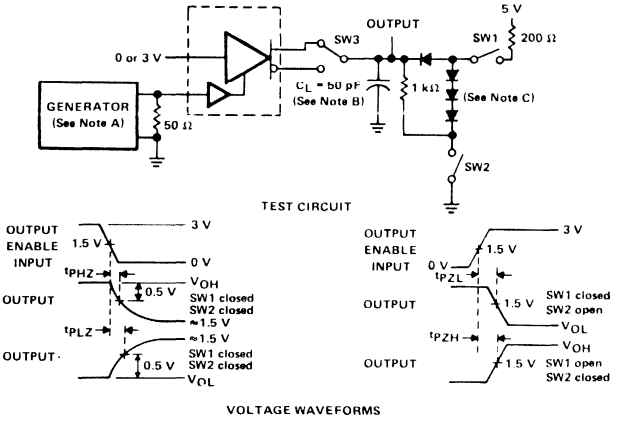


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

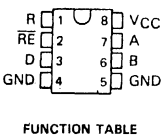
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

SN65076B, SN75076B
DIFFERENTIAL BUS TRANSCEIVERS

JANUARY 1990

- Bidirectional Transceiver
- Designed for Multipoint Transmission In Noisy Environments Such as Automotive Applications
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±10 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE
(DRIVER)

INPUT	OUTPUTS	
D	A	B
H	H	L
L	L†	H†

†These levels assume that the open-collector outputs (A) and the open-emitter outputs (B) are connected to a pullup and pull-down resistor, respectively.

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	L
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	H
X	H	Z

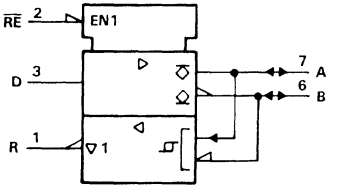
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN65076B and SN75076B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for noisy environments, where a low-impedance termination to ground is required.

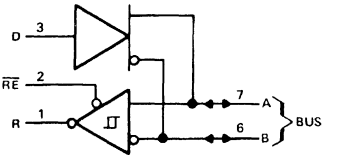
The SN65076B and SN75076B combine a differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The receiver has an active-low enable. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

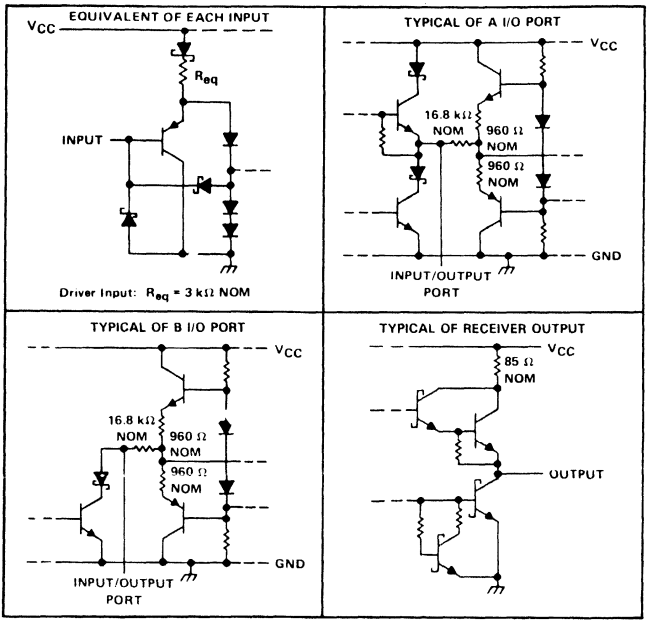


TEXAS INSTRUMENTS

description (continued)

The driver is designed to handle loads up to 10 mA of sink and source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C in the P package and 170°C in the D package. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65076B is characterized for operation from −40°C to 105°C and the SN75076B is characterized for operation from 0°C to 70°C.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65076B . . . . . −40°C to 105°C
SN75076B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

			MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12	V
					−7	
High-level input voltage, V_{IH}	D and $\overline{RE}$		2			V
Low-level input voltage, V_{IL}	D and $\overline{RE}$				0.8	V
Differential input voltage, V_{ID} (see Note 2)					±12	V
High-level output current, I_{OH}	Driver (A)				−10	mA
	Receiver				−400	μA
Low-level output current, I_{OL}	Driver (B)				10	mA
	Receiver				8	
Operating free-air temperature, T_A	SN65076B		−40		105	°C
	SN75076B		0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	V_I = 2 V, I_O = 0		0		6	V
V_{OD1}	Differential output voltage	I_O = 0		1.5		6	V
V_{OD2}	Differential output voltage	See Figure 1		1.5		5	V
I_O	Output current	V_I = 0.8 V	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load				30	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Differential-output turn-on time	See Figure 3		60	90	ns
t_{off}	Differential-output turn-off time			75	110	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§			50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, I_{OH} = −400 μA, See Figure 2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 2			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V			±20	μA
I_I	Line input current	Other input = 0 V, V_I = 12 V See Note 3 V_I = −7 V			1 −0.8	mA
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V			20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V			−100	μA
r_i	Input resistance		12			kΩ
I_{OS}	Short-circuit output current		−15		−85	mA
I_{CC}	Supply current (total package)	No load			30	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 3: This applies for both power on and power off.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V, C_L = 15 pF, See Figure 4		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 5		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 5		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

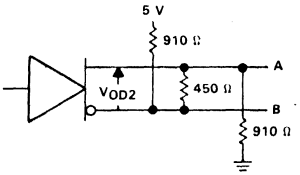


FIGURE 1. DRIVER V_{OD2}

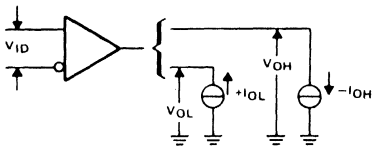
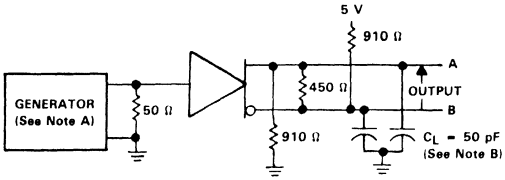
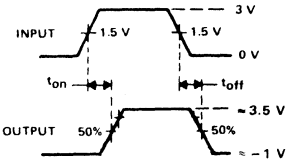


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

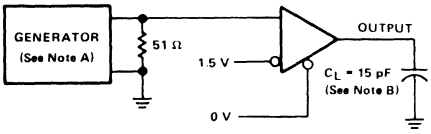


TEST CIRCUIT

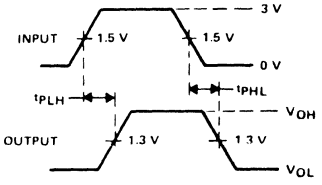


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

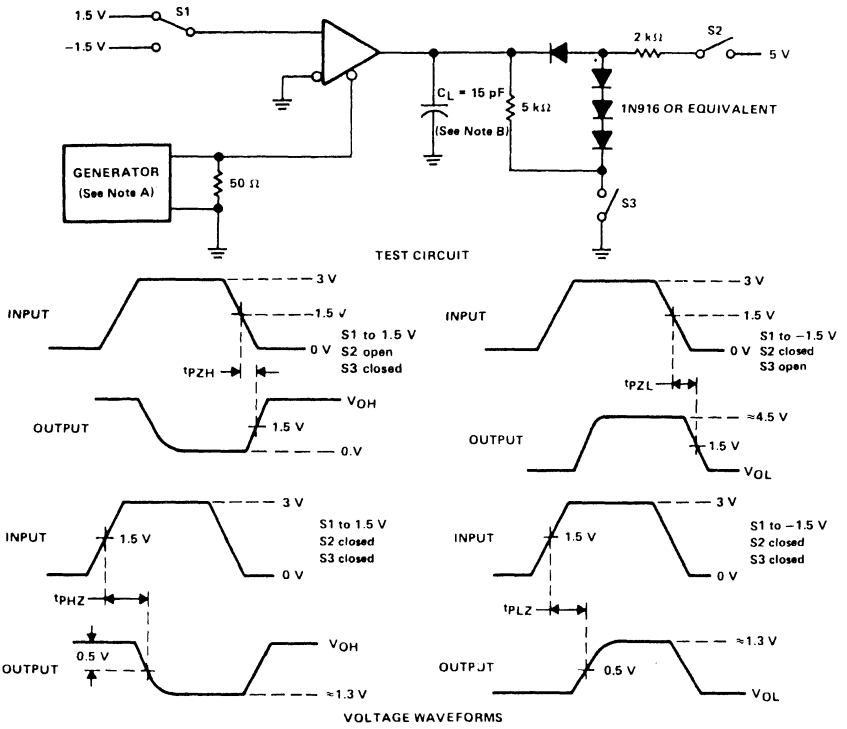


FIGURE 5. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

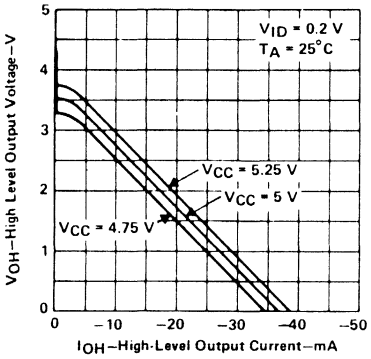


FIGURE 6

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

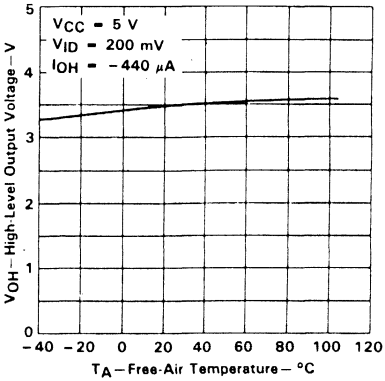


FIGURE 7

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

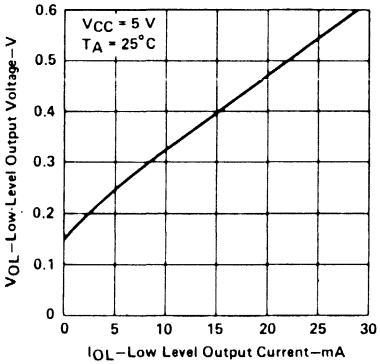


FIGURE 8

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

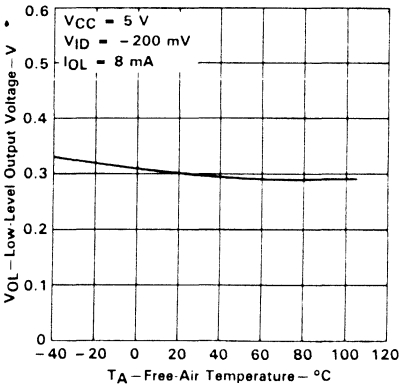


FIGURE 9

TYPICAL CHARACTERISTICS

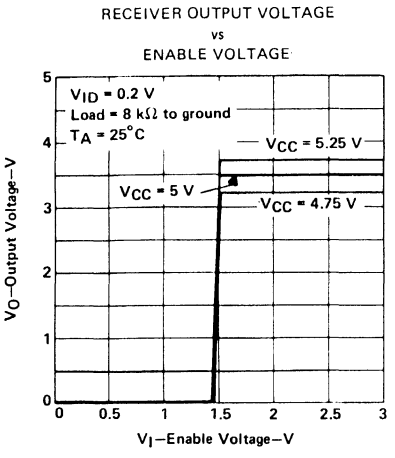


FIGURE 10

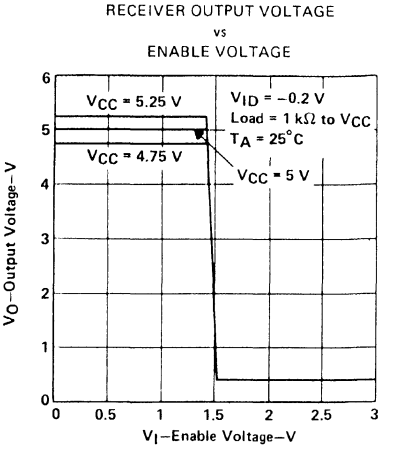


FIGURE 11

TYPICAL APPLICATION

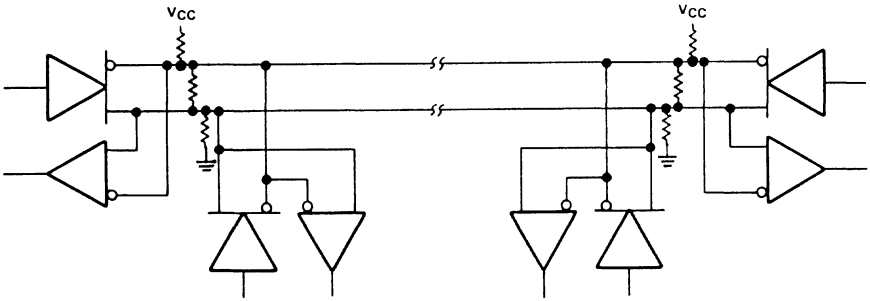


FIGURE 12. TYPICAL APPLICATION CIRCUIT

- **Meets EIA Standards RS-422-A, RS485**
- **Meets CCITT Recommendations V.10, V.11, X.26, X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Driver Common-Mode Output Voltage Range of −7 V to 12 V**
- **Driver Positive- and Negative-Current Limiting**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of −12 V to 12 V**
- **Receiver Input Sensitivity ... ±200 mV**
- **Receiver Hysteresis ... 50 mV Typ**
- **Receiver High-Input-Impedance ... 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN751177 Only**
- **Operates from Single 5-V Supply**

description

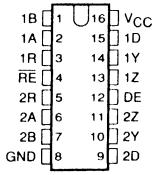
The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 M bits per second. They are designed to improve the performance of full-duplex data communications over long bus lines and meet EIA standards RS-422-A, RS-485 and several CCITT recommendations.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on the transmission bus line.

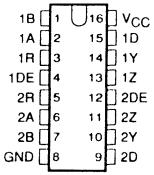
The receiver features high input impedance of 12 kΩ, an input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V and typical input hysteresis of 50 mV. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs will always be high.

The SN751177 and SN751178 are characterized for operation from −20°C to 85°C.

SN751177
N PACKAGE
(TOP VIEW)



SN751178
N PACKAGE
(TOP VIEW)



SN751177, SN751178
FUNCTION TABLE OF EACH DRIVER

INPUT	ENABLE	OUTPUT	
D	DE	Y	Z
H	H	H	L
L	L	L	H
X	X	Z	Z

SN751177
FUNCTION TABLE OF EACH RECEIVER

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	H	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	L
$V_{ID} \geq -0.2$ V	X	X
X	H	Z

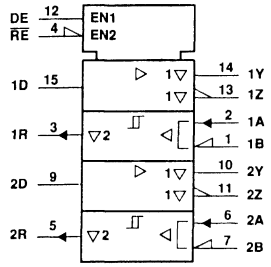
SN751178
FUNCTION TABLE OF EACH RECEIVER

DIFFERENTIAL INPUTS A − B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	?
$V_{ID} \geq -0.2$ V	L

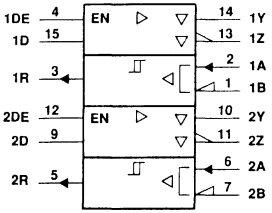
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbols†

SN751177



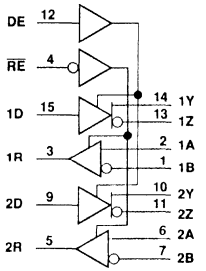
SN751178



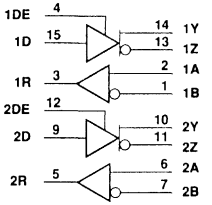
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagrams (positive logic)

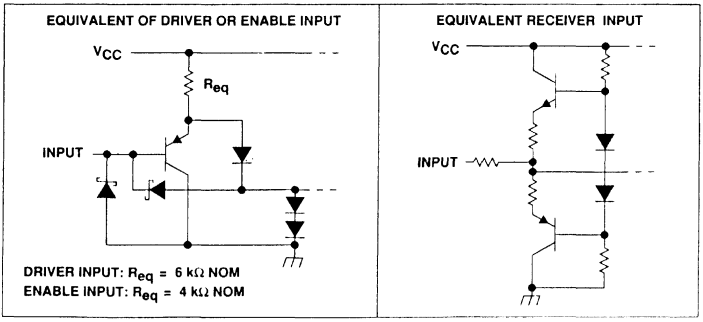
SN751177



SN751178

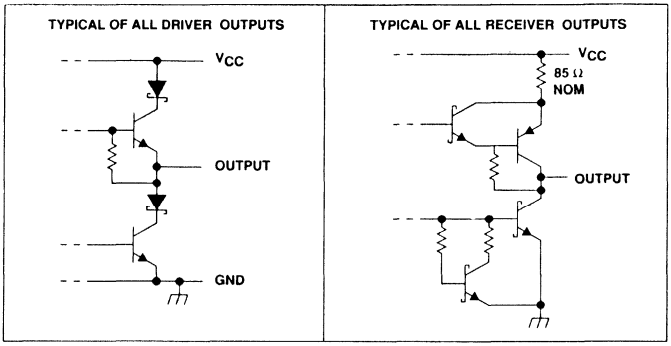


schematics of inputs



All resistor values are nominal.

schematics of outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, DE, $\overline{RE}$, and D inputs . . . . . 7 V
Input voltage range, receiver A or B inputs . . . . . −25 V to 25 V
Receiver differential input voltage range (see Note 2) . . . . . −25 V to 25 V
Output voltage range,Driver . . . . . −10 V to 15 V
Receiver low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values,except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, and D inputs	2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC} (see Note 4)	Driver	−7		12	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Common-mode input voltage, V_{IC}	Receiver			±12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		−20		85	°C

NOTE 4: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

DRIVER SECTIONS

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA			1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		2			V
				1/2 V_{OD1}			
		R_L = 54 Ω, See Figure 1		1.5		5	
V_{OD3}	Differential output voltage	See Note 5		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 6)	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage (see Note 4)			−1		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 6)					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				−100	mA
I_{OS}	Short-circuit output current (see Note 7)	V_O = −7 V				−250	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	outputs enabled		80	110	μA
			outputs disabled		50	80	

†All typical values are at V_{CC} = 5 V and T_A = 25°C

NOTES: 4. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
5. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
6. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
7. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

driver switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		20	25	ns
t_{TD}	Differential output transition time			27	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω, C_L = 50 pF, See Figure 4		20	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 5		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 6		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 5		90	120	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 6		30	45	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422A	RS-485
$\|V_{OD1}\|$	V_O	V_O
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{OS}\|$	$\|V_{OS}\|$
$\Delta\|V_{OC}\|$	$\|V_{OS} - \overline{V}_{OS}\|$	$\|V_{OS} - \overline{V}_{OS}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTIONS

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential input low threshold voltage (see Note 4)		V_O = 0.5 V,	I_O = 16 mA	−0.2			V
V_{hys}	Input hysteresis (see Note 8)					50		mV
V_{IK}	Enable clamp voltage	SN751177	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	SN751177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 9)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	SN751177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	SN751177	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current (see Note 7)				−15		−85	mA
I_{CC}	Supply current		No load,	outputs enabled		80	110	mA
r_i	Input resistance				12			kΩ

†All typical values are at V_{CC} = 5 V and T_A = 25°C

NOTES: 4. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

7. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
8. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
9. Refer to EIA standards RS-422-A, RS-423-A, RS-485-A for exact conditions.

receiver switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		V_{ID} = −1.5 V to 1.5 V,			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output		C_L = 15 pF,	See Figure 7		22	35	ns
t_{PZH}	Output enable time to high level	SN751177	C_L = 15 pF,	See Figure 8		17	25	ns
t_{PZL}	Output enable time to low level					20	27	ns
t_{PHZ}	Output disable time from high level					25	40	ns
t_{PLZ}	Output disable time from low level					30	40	ns

PARAMETER MEASUREMENT INFORMATION

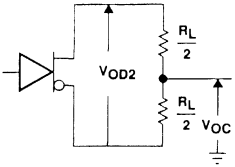


FIGURE 1. DRIVER TEST CIRCUIT, V_{OD} AND V_{OC}

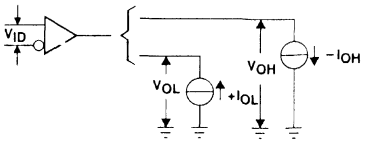
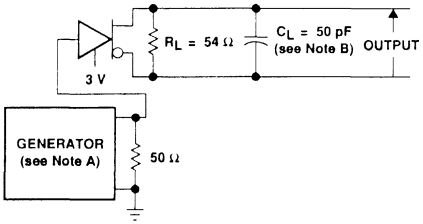
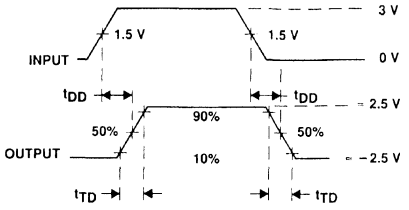


FIGURE 2. RECEIVER TEST CIRCUIT, V_{OH} AND V_{OL}

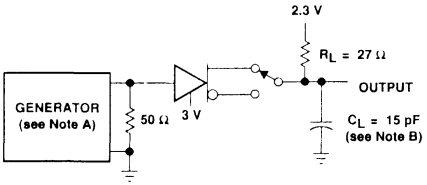


(a) DRIVER TEST CIRCUIT

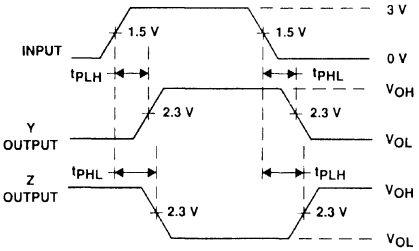


(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL OUTPUT DELAY AND TRANSITION TIMES



(a) DRIVER TEST CIRCUIT

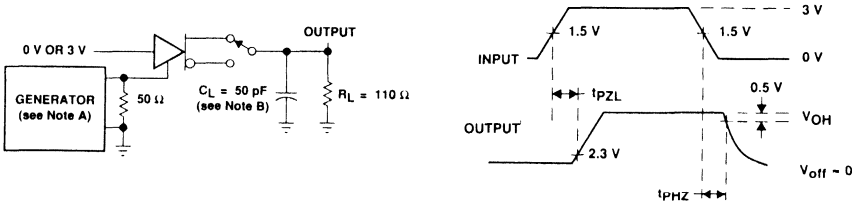


(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 4. DRIVER PROPAGATION DELAY TIMES

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns..
B. C_L includes probe and jig capacitance.

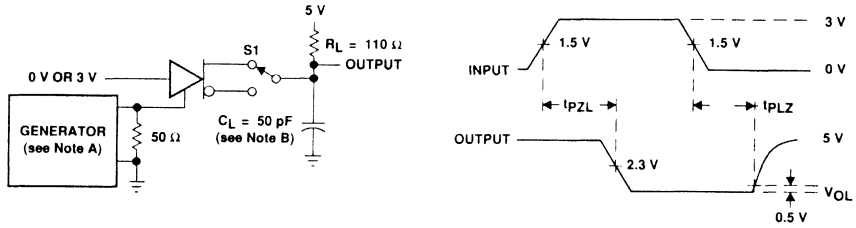
PARAMETER MEASUREMENT INFORMATION



(a) DRIVER TEST CIRCUIT

(b) DRIVER VOLTAGE WAVEFORMS

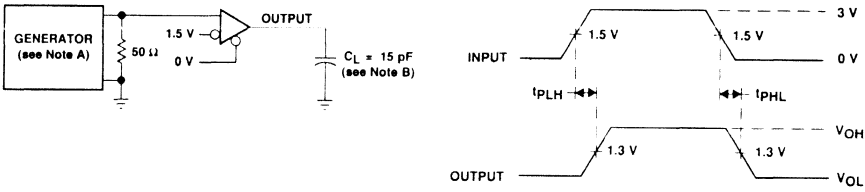
FIGURE 5. DRIVER ENABLE AND DISABLE TIMES



(a) DRIVER TEST CIRCUIT

(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 6. DRIVER ENABLE AND DISABLE TIMES



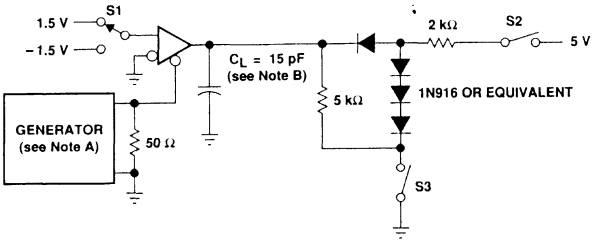
(a) RECEIVER TEST CIRCUIT

(b) RECEIVER VOLTAGE WAVEFORMS

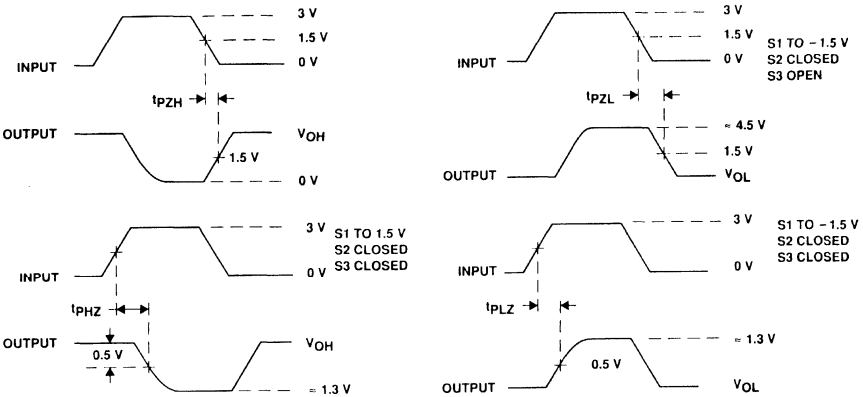
FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



(a) RECEIVER TEST CIRCUIT



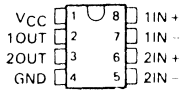
(b) RECEIVER VOLTAGE WAVEFORMS

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

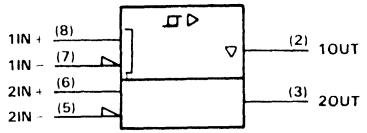
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns..
B. C_L includes probe and jig capacitance..

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets EIA Standards RS-232 and CCITT V.28 with External Components**
- **Meets Federal Standards 1020 and 1030**
- **Built-in 5-MHz Low-Pass Filter**
- **Operates from Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **8-Pin Dual-In-Line Package**
- **Pinout Compatible with the μA9637 and μA9639**

D, JG, OR P PACKAGE
(TOP VIEW)

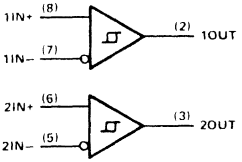


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

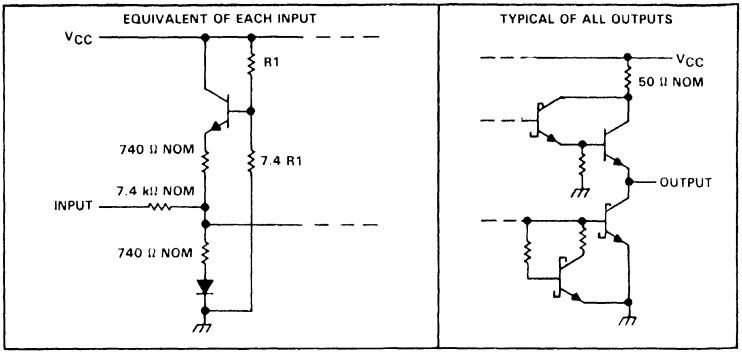


description

The SN75146 is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A. The receiver is designed to have a constant impedance with input voltages of ±3 volts to ±25 volts allowing it to meet the requirements of EIA standard RS-232-C and CCITT recommendation V.28 with the addition of an external bias resistor. This receiver is designed for low-speed operation below 355 kilohertz, and has a built-in 5-megahertz low-pass filter to attenuate high-frequency noise. The inputs are compatible with either a single-ended or a differential line system and the outputs are TTL compatible. This device operates from a single 5-volt power supply and is supplied in both the 8-pin dual-in-line and small outline packages.

The SN75146 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, and the P package to 640 mW at 70°C at the rate of 8 mW/°C. The SN75146 chips are glass mounted in the JG package.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			+7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

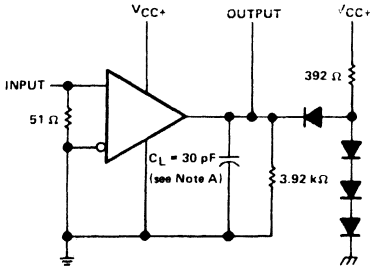
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	See Note 4		−0.2‡		0.2	V
				−0.4‡		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			70			mV
V_{IB}	Input bias voltage	I_I = 0		2		2.4	V
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
r_i	Input resistance	See Note 5,	V_I = 3 V to 25 V or V_I = −3 V to −25 V	6	7.8	9.5	kΩ
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 6	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V	No load		35	60	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 4. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
5. r_i is defined by $\Delta V_I/\Delta I_I$.
6. The input not under test is grounded.

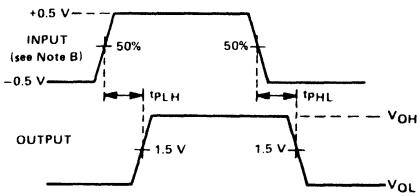
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1	100	150	300	ns
t_{PHL}	Propagation delay time, high-to-low-level output		100	150	300	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 300 kHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

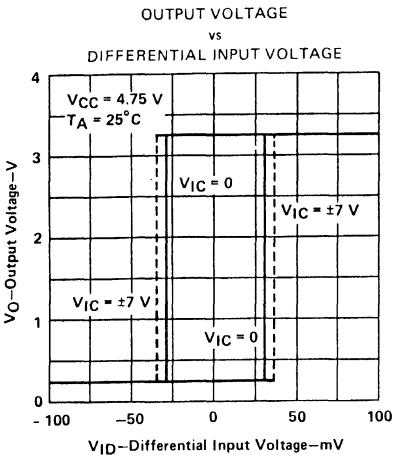


FIGURE 2

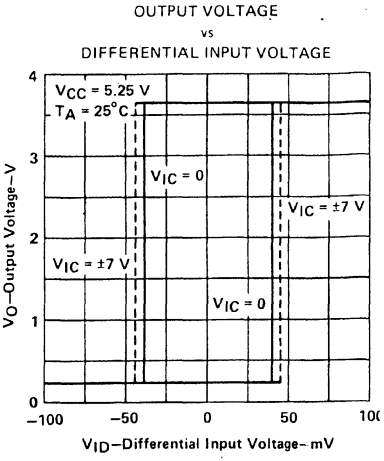
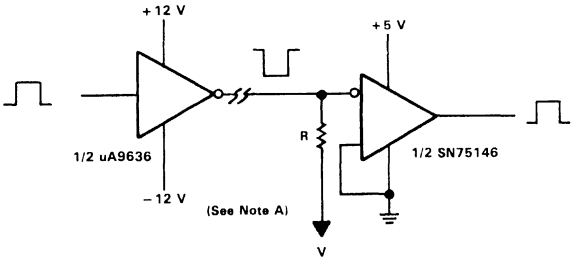


FIGURE 3

TYPICAL APPLICATION DATA



NOTE A: In order to meet the input-impedance and open-circuit-input voltage requirements of RS-232-C and CCITT V.28 and guarantee open-circuit-input failsafe operation, R and V are selected to satisfy the following equations:

$$V = -1.1 - 3.3\,\frac{R}{r_i} \text{ volts}$$

$$3\text{ k}\Omega \le \frac{R(r_i)}{R + r_i} \le 7\text{ k}\Omega$$

FIGURE 4. RS-232-C SYSTEM APPLICATIONS

TYPICAL APPLICATION DATA

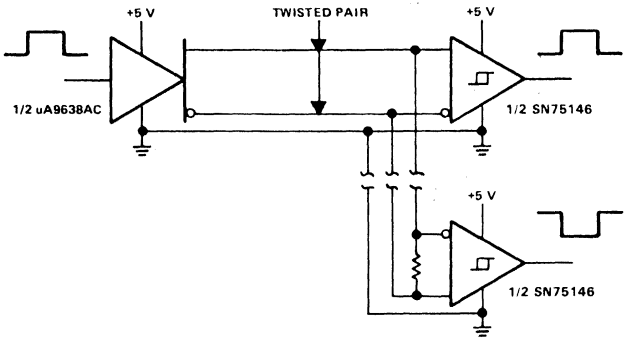


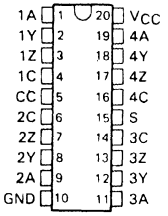
FIGURE 5. RS-422-A SYSTEM APPLICATIONS

SN75151, SN75153
QUAD DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

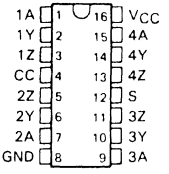
OCTOBER 1986

- **Meets EIA Standard RS-422-A**
- **High-Impedance Output State for Party-Line Operation**
- **High Output Impedance in Power-Off Condition**
- **Low Input Current to Minimize Loading**
- **Single 5-V Supply**
- **40-mA Sink- and Source-Current Capability**
- **High-Speed Schottky Circuitry**
- **Low Power Requirements**

SN75151
DW, J, OR N PACKAGE
(TOP VIEW)



SN75153
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These line drivers are designed to provide differential signals with high current capability on balanced lines. These circuits provide strobe and enable inputs to control all four drivers, and the SN75151 provides an additional enable input for each driver. The output circuits have active pull-up and pull-down and are capable of sinking or sourcing 40 milliamperes.

The SN75151 and SN75153 meet all requirements of EIA Standard RS-422-A and Federal Standard 1020. They are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

SN75151

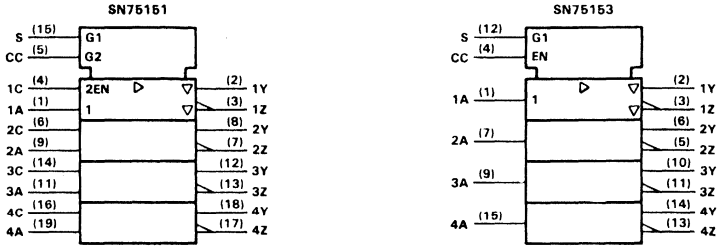
INPUTS				OUTPUTS	
ENABLE CC	ENABLE C	STROBE S	DATA A	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

SN75153

INPUTS			OUTPUTS	
ENABLE CC	STROBE S	DATA A	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

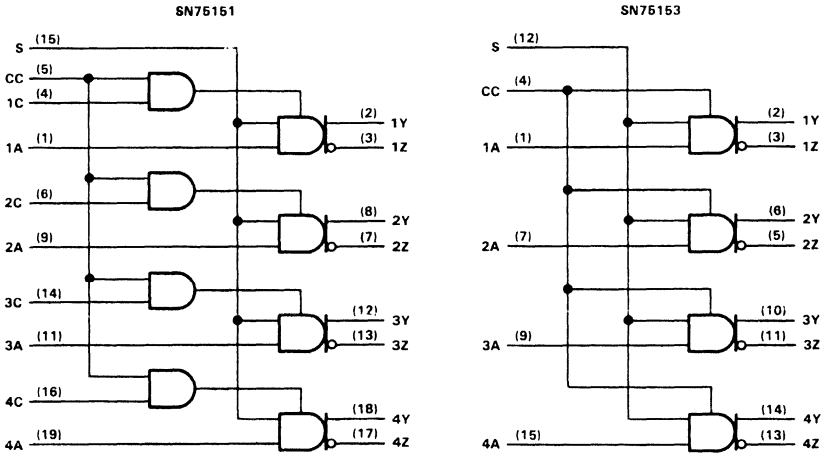
TEXAS INSTRUMENTS

logic symbols†

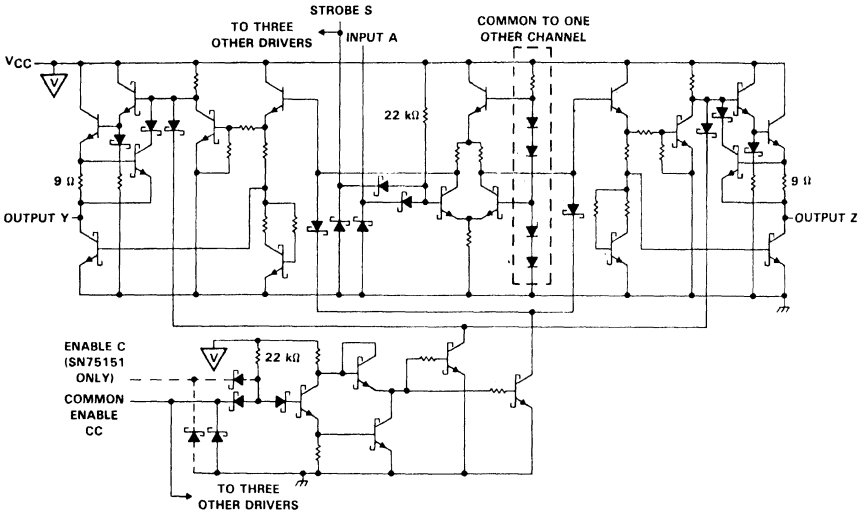


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



schematic



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package at the rate of 9 mW/°C, the J package at the rate of 8.2 mW/°C, and the N package at the rate of 9.2 mW/°C. In the J package, the chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	−0.25		6	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA	CC, S			−2	V
			All others		−0.9	−1.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −20 mA	2.5			V
			I_{OH} = −40 mA	2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = MAX, I_{OL} = 40 mA			0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.4	$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	2.8		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.01	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.8	3	V
		V_{CC} = MIN			1.6	3	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Enable at 0.8 V	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
			V_O = V_{CC}			20	
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	C('151), A			20	μA
			CC, S			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	C ('151), A			−0.36	mA
			CC,S			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−50	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load	Outputs disabled		30	60	mA
			Outputs enabled		60	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 2, Termination B		13	26	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		12	20	ns
t_{THL}	Transition time, high-to-low-level output			12	20	ns
t_{PZH}	Outut enable time to high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		18	35	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		20	35	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		19	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		13	30	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

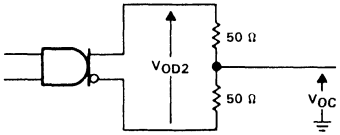
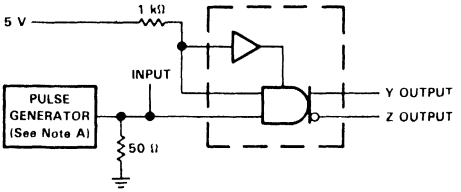
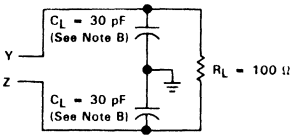


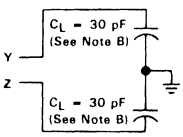
FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

PARAMETER MEASUREMENT INFORMATION

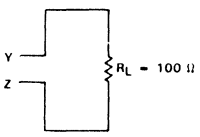




TERMINATION A

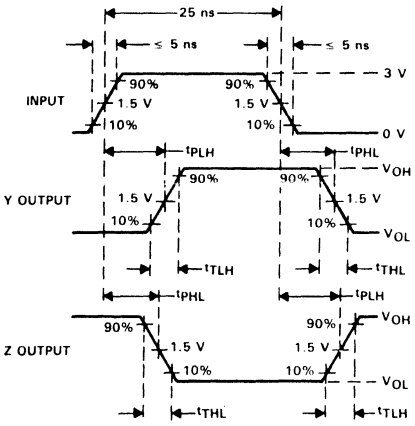


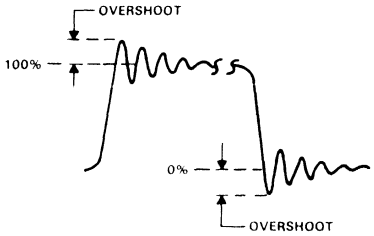
TERMINATION B



TERMINATION C

TEST CIRCUITS



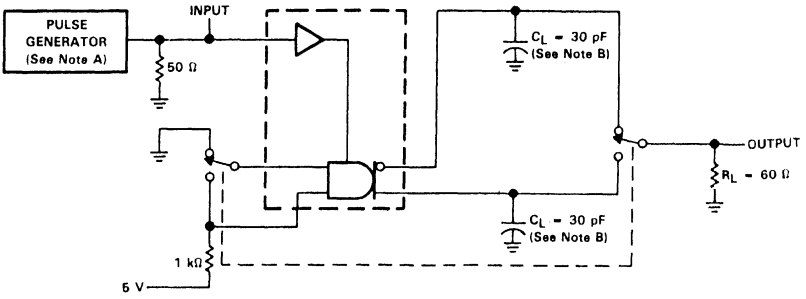


VOLTAGE WAVEFORMS

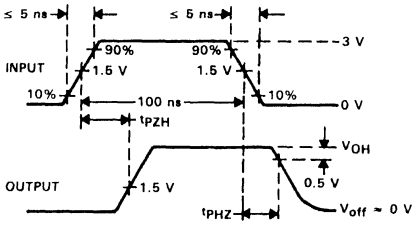
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

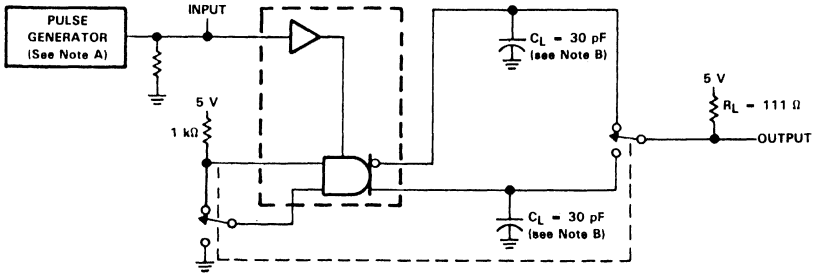


VOLTAGE WAVEFORMS

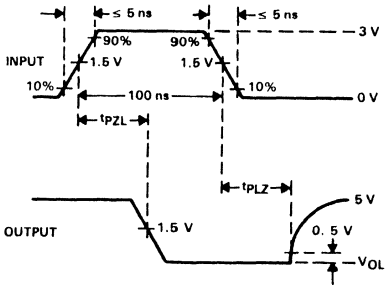
FIGURE 3. t_{PZH} AND t_{PHZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

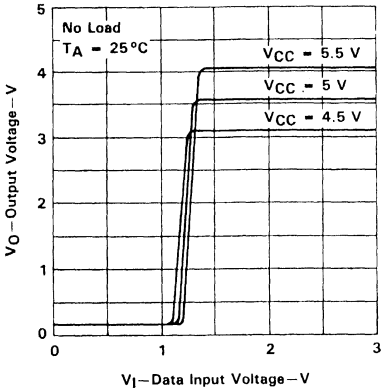


FIGURE 5

Y OR Z OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

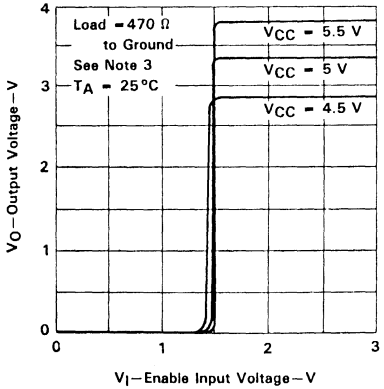


FIGURE 6

Y OR Z OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

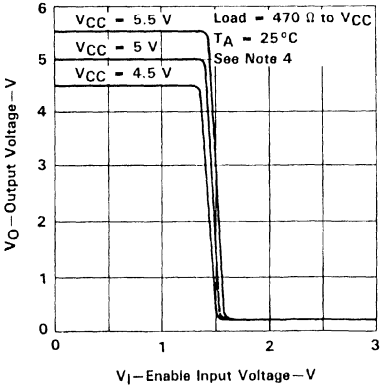


FIGURE 7

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

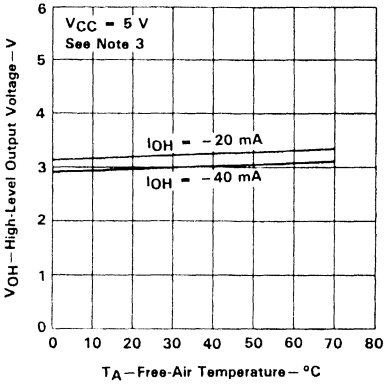


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

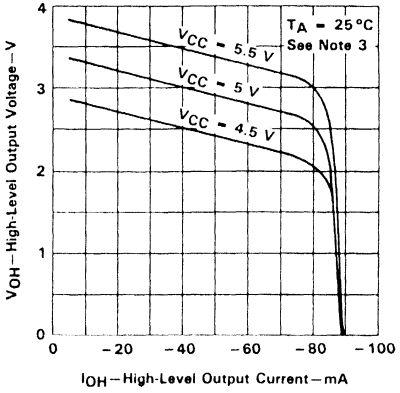


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

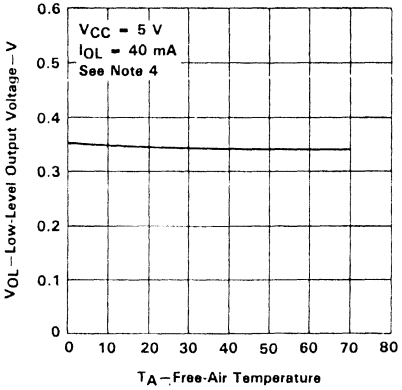


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

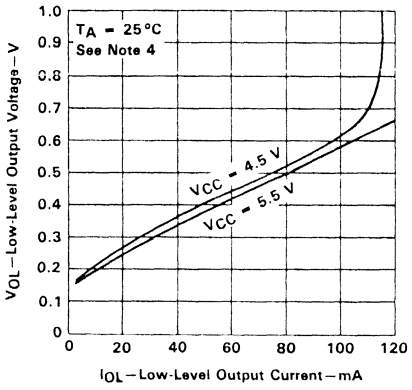


FIGURE 11

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

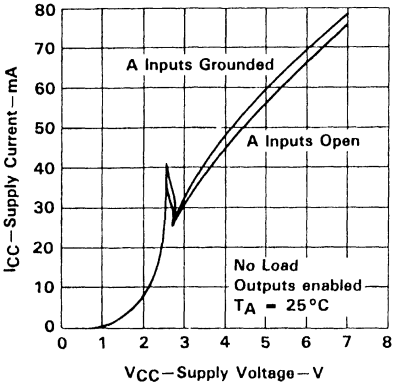


FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

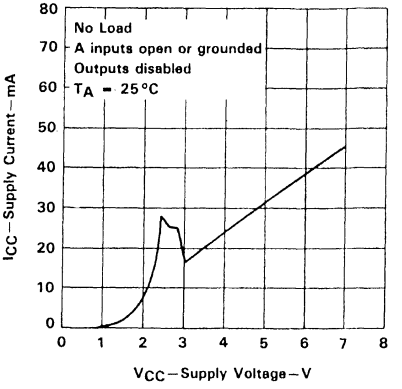
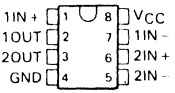


FIGURE 13

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package
- Similar to uA9637AC except for Corner V_{CC} and Ground Pin Positions

SN55157 . . . JG PACKAGE
SN75157 . . . D, JG, OR P PACKAGE
(TOP VIEW)

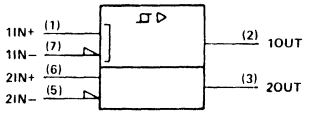


description

The SN75157 is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and small outline package.

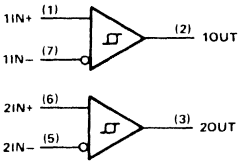
The SN55157 is characterized over the full military temperature range of −55°C to 125°C. The SN75157 is characterized for operation from 0°C to 70°C.

logic symbol†

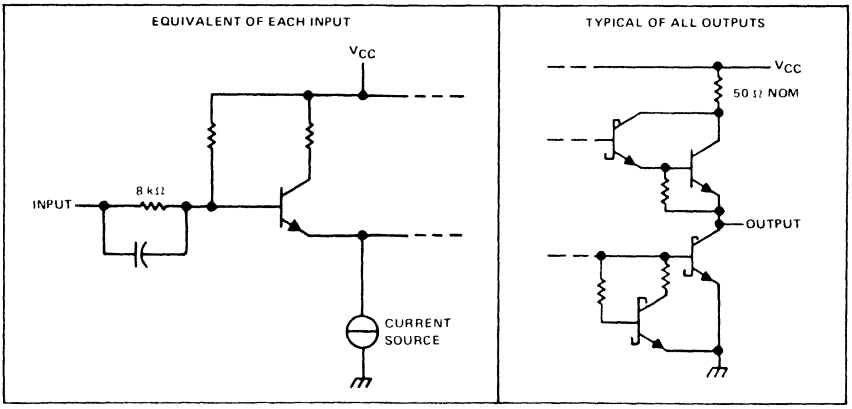


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
SN55157 JG package . . . . . 1050 mW
SN75157 D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range: SN55157 . . . . . −55°C to 125°C
SN75157 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the SN55157 JG package to 672 mW at 70°C at the rate of 8.4 mW/°C, the SN75157 JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN55157 chips are alloy mounted and SN75157 chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±7	V
Operating free-air temperature, T_A	SN55157	−55	25	125	°C
	SN75157	0	25	70	

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

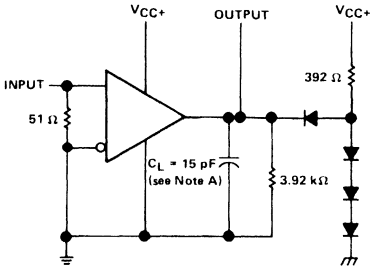
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

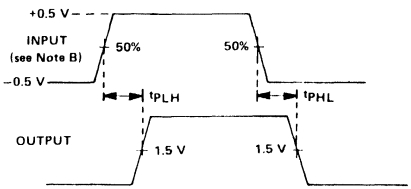
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

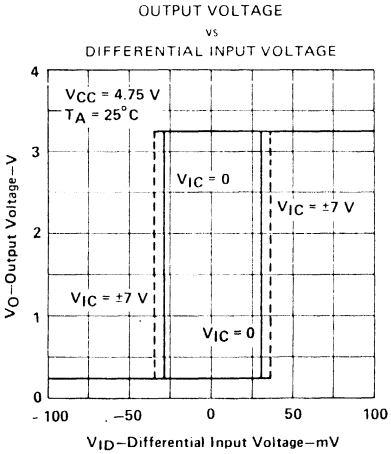


FIGURE 2

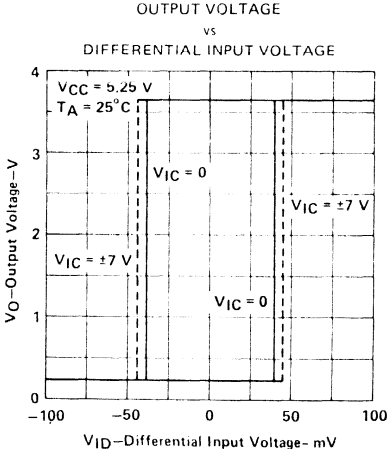


FIGURE 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

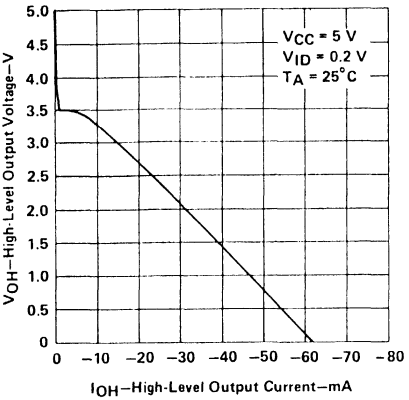


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

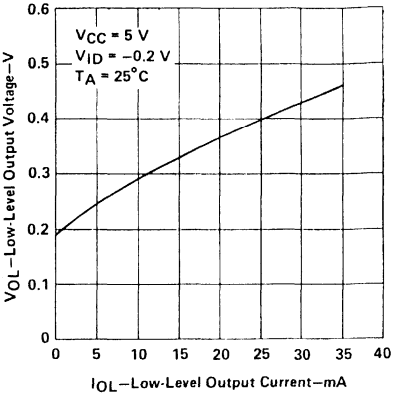


FIGURE 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

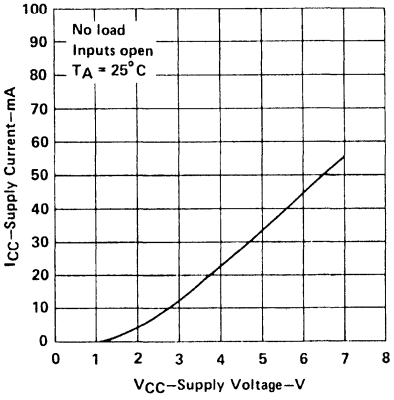


FIGURE 6

TYPICAL APPLICATION DATA

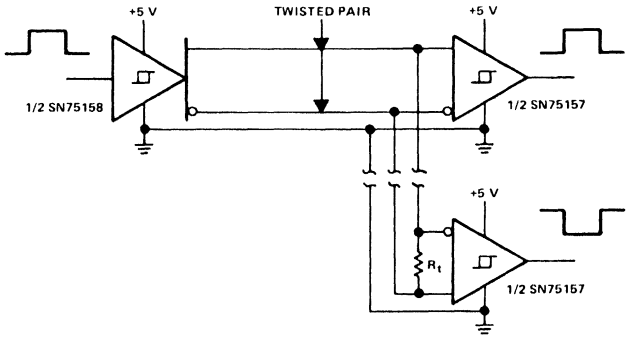


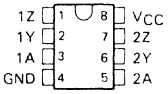
FIGURE 7. RS-422-A SYSTEM APPLICATIONS

SN55158, SN75158
DUAL DIFFERENTIAL LINE DRIVERS

SEPTEMBER 1986

- Meets EIA Standard RS-422-A
- Single 5-V Supply
- Balanced-Line Operation
- TTL-Compatible
- High Output Impedance in Power-Off Condition
- High-Current Active-Pullup Outputs
- Short-Circuit Protection
- Dual Channels
- Input Clamp Diodes

SN55158 . . . JG PACKAGE
SN75158 . . . D, JG, OR P PACKAGE
(TOP VIEW)

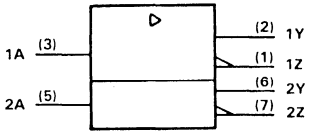


description

The SN55158 and SN75158 are dual complementary-output line drivers designed to satisfy the requirements set by the EIA Standard RS-422-A interface specifications. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

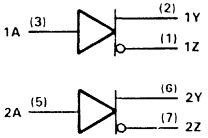
The SN55158 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75158 is characterized for operation from 0°C to 70°C.

logic symbol†



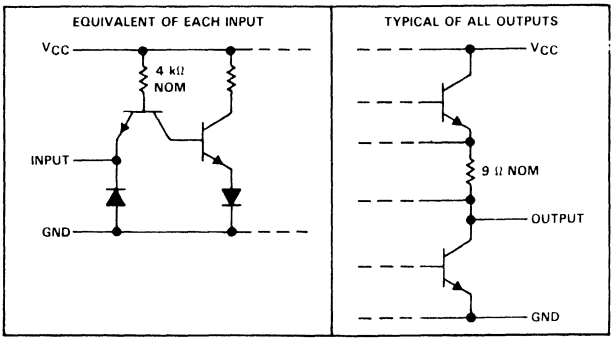
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55158 . . . . . −55°C to 125°C
SN75158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.
2. In the JG package, SN55158 chips are alloy mounted and SN75158 chips are glass mounted

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	N/A
JG (SN55158)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (SN75158)	825 mW	6.6 mW/°C	528 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	N/A

recommended operating conditions

	SN55158			SN75158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN55158			SN75158			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA		2	3.0		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.2	0.4		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0			3.5	$2V_{OD2}$		3.5	$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN		R_L = 100 Ω, See Figure 1	2	3.0		2	3.0		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	V_{CC} = MIN				±0.02	±0.4		±0.02	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX				1.9	3		1.8	3	V
		V_{CC} = MIN				1.4	3		1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX				±0.01	±0.4		±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100		0.1	100	μA
			V_O = −0.25 V			0.1	100		0.1	100	
			V_O = −0.25 to 6 V				±100			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
I_{OS}	Short-circuit output current#	V_{CC} = MAX			−40	−90	−150	−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load,	Inputs grounded, T_A = 25°C			37	50		37	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55158			SN75158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination A		16	25		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20		10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination B		13	20		13	20	ns
t_{PHL}	Propagation delay time, high-to-low level output			9	15		9	15	ns
t_{TLH}	Transition time, low-to-high-level output	See Figure 2, Termination A		4	20		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20		4	20	ns
	Overshoot factor	See Figure 2, Termination C			10			10	%

PARAMETER MEASUREMENT INFORMATION

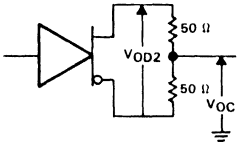
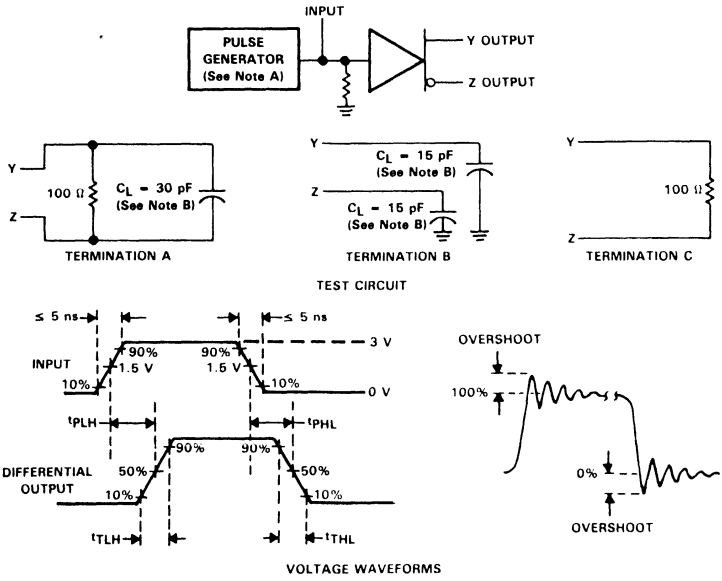


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 25 ns, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

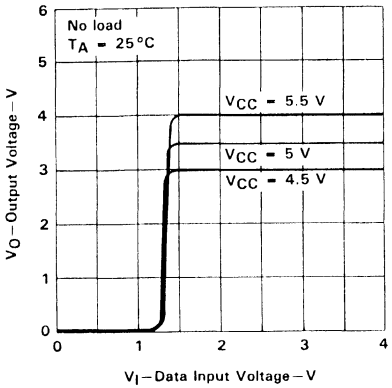


FIGURE 3

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

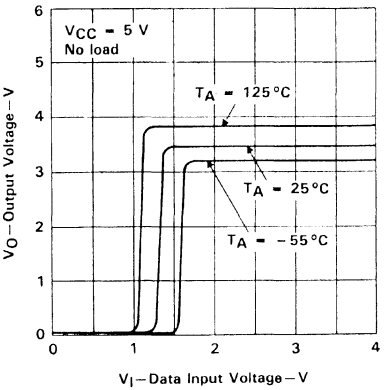


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

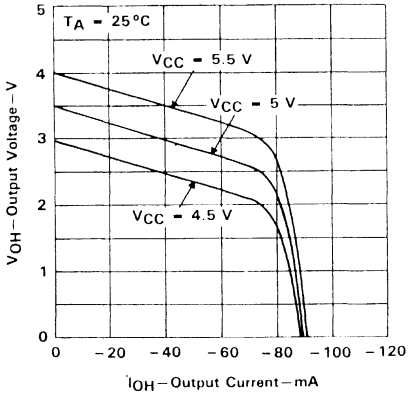


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

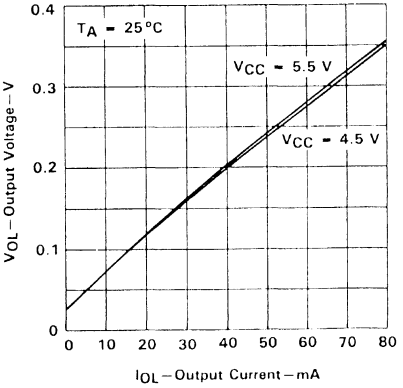


FIGURE 6

†Data for temperatures below 0°C and above 70°C are applicable to SN55158 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

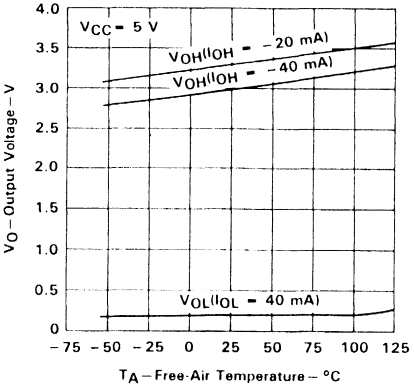


FIGURE 7

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

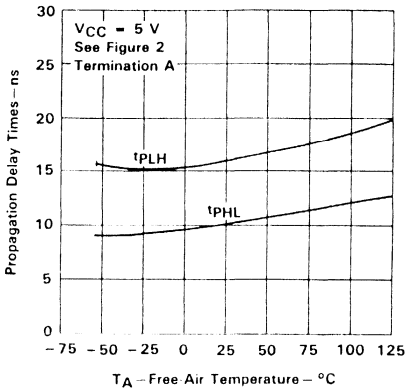


FIGURE 8

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

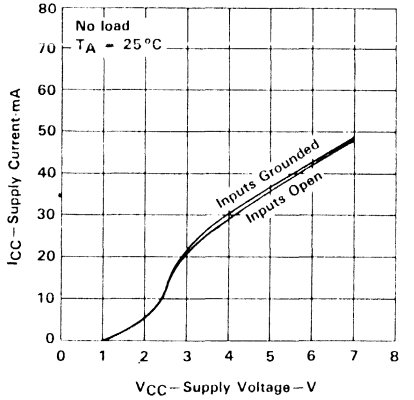


FIGURE 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

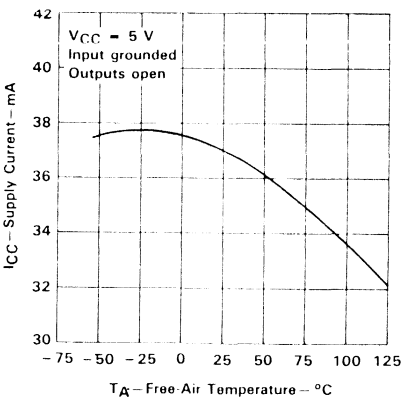


FIGURE 10

†Data for temperatures below 0°C and above 70°C are applicable to SN55158 circuits only.

TYPICAL CHARACTERISTICS

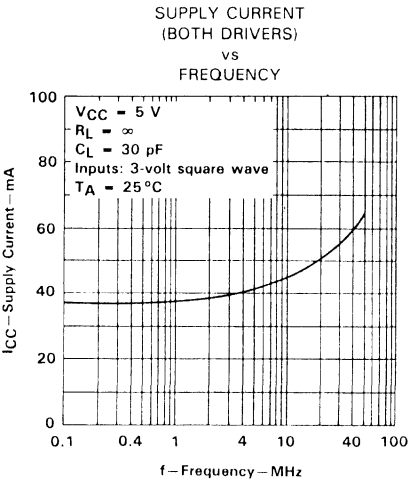


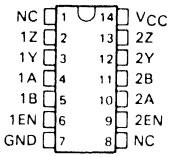
FIGURE 11

DUAL DIFFERENTIAL LINE DRIVERS WITH 3 STATE OUTPUTS

SEPTEMBER 1986

- **Meets EIA Standard RS-422-A**
- **Single 5-V Supply**
- **Balanced Line Operation**
- **TTL-Compatible**
- **High-Impedance Output State for Party-Line Applications**
- **High-Current Active-Pull-Up Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Clamp Diodes at Inputs**

D, J, OR N PACKAGE
(TOP VIEW)



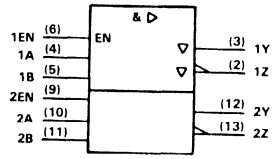
NC – No internal connection

description

The SN75159 dual differential line driver with three-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

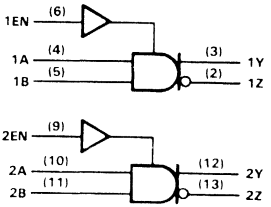
The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†

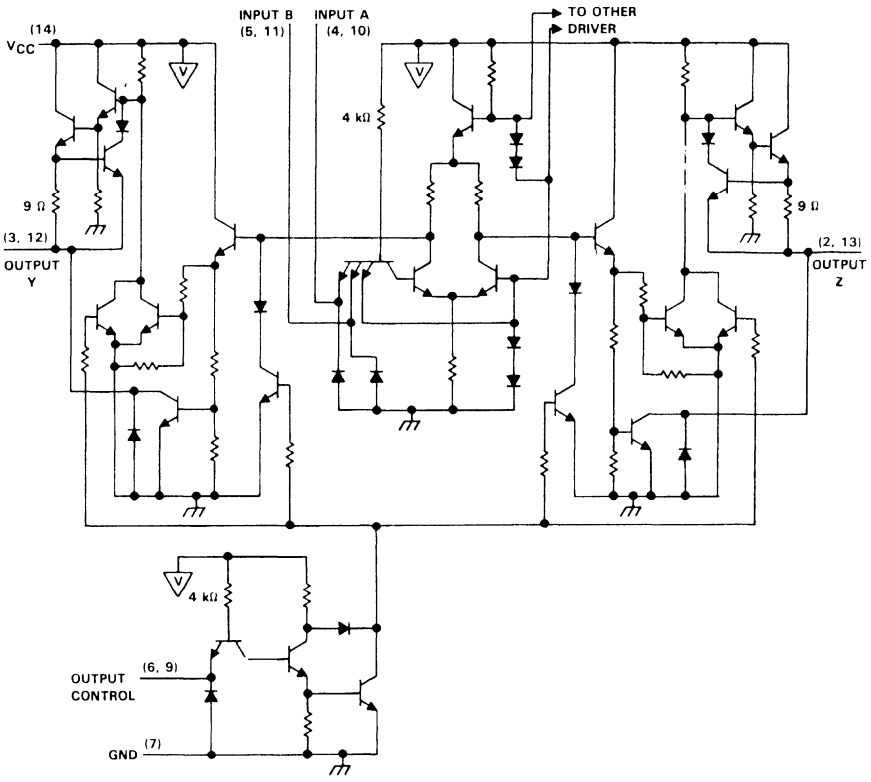


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



▽ . . . V_{CC} bus

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state voltage applied to open-collector outputs . . . . . 12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to the network ground terminal. V_{OD} is at the Y output with respect to the Z output.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75159 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output voltage, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OH} = −40 mA			2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OL} = 40 mA				0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = 5.25 V, I_O = −40 mA				−1.1	−1.5	V
V_O	Output voltage	V_{CC} = 4.75 V to 5.25 V, I_O = 0			0		6	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				3.5	$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 4.75 V			2	3.0		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	V_{CC} = 4.75 V	R_L = 100 Ω, See Figure 1			±0.02	±0.4	V
V_{OC}	Common-mode output voltage§	V_{CC} = 5.25 V	R_L = 100 Ω, See Figure 1			1.8	3	V
		V_{CC} = 4.75 V	R_L = 100 Ω, See Figure 1			1.5	3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡	V_{CC} = 4.75 V to 5.25 V	R_L = 100 Ω, See Figure 1			±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	μA
			V_O = −0.25 V			−0.1	−100	μA
			V_O = −0.25 V to 6 V				±100	μA
I_{OZ}	Off-state (high impedance-state) output current	V_{CC} = 5.25 V, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10	μA
			T_A = 70°C	V_O = 0			−20	μA
				V_O = 0.4 V			±20	μA
				V_O = 2.4 V			±20	μA
				V_O = V_{CC}			20	μA
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V				−1	−1.6	mA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	VCC = 5.25 V, T_A = 25°C	Inputs grounded, No load,			47	65	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

† All typical values are at T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

PARAMETER MEASUREMENT INFORMATION

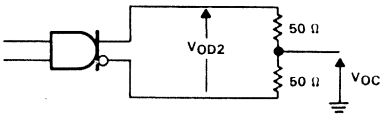
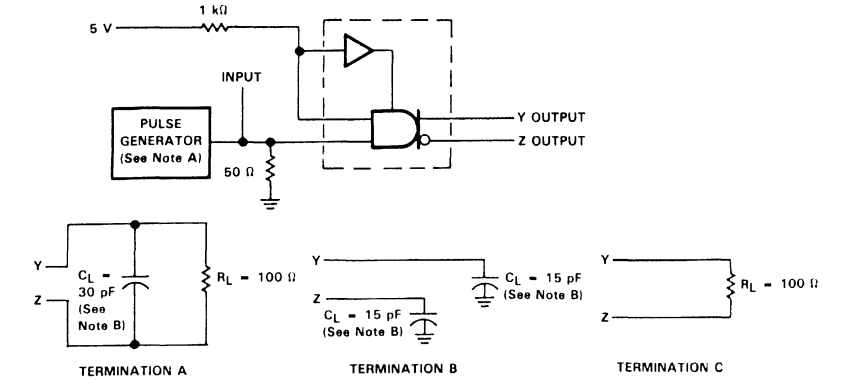
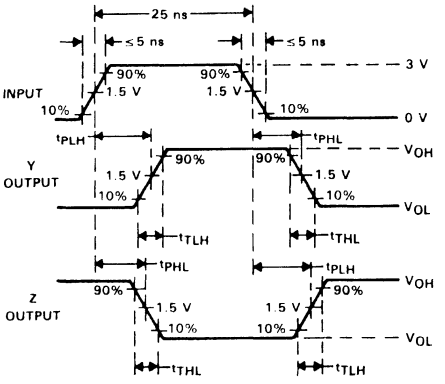
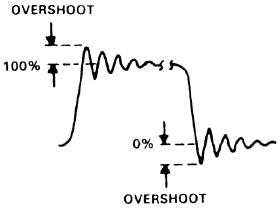


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

PARAMETER MEASUREMENT INFORMATION



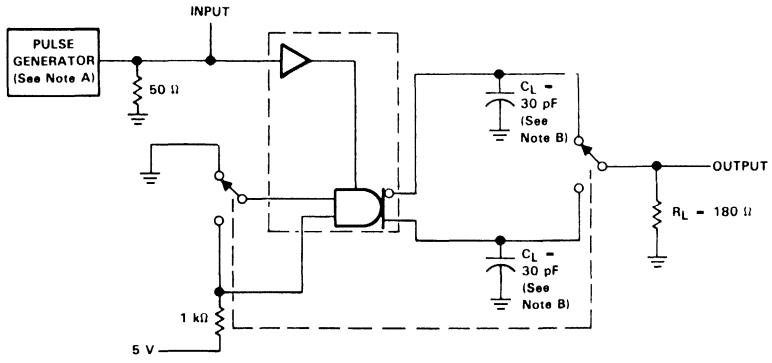




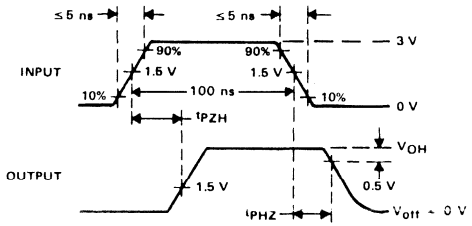
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

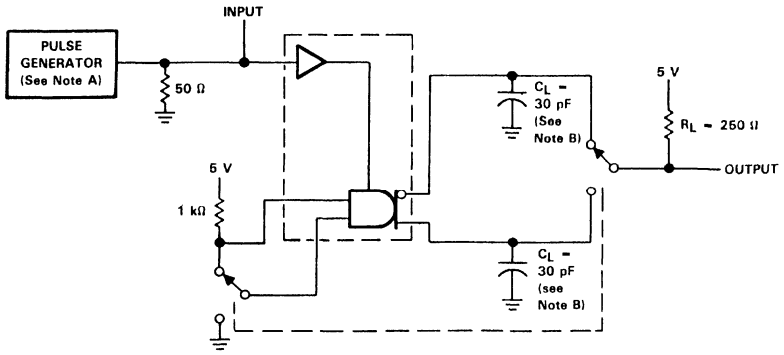


VOLTAGE WAVEFORMS

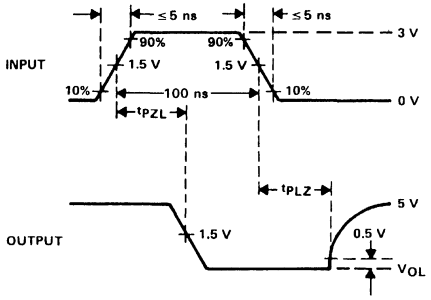
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz
B. C_L includes probe and jig capacitance.

FIGURE 3. t_{PZH} AND t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz.
C. C_L includes probe and jig capacitance.

FIGURE 4. t_{PZL} AND t_{PLZ}

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

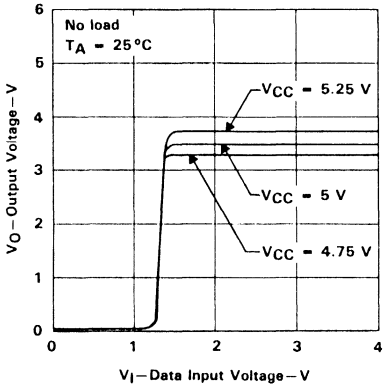


FIGURE 5

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

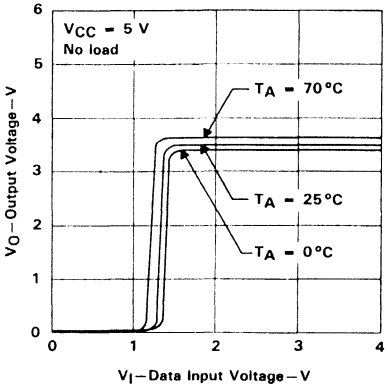


FIGURE 6

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

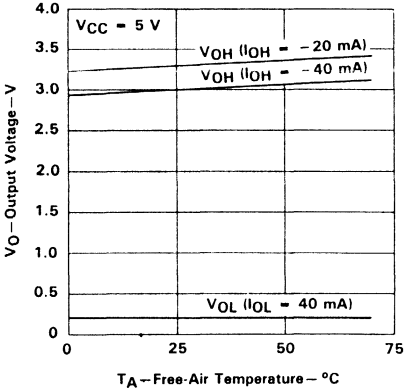


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

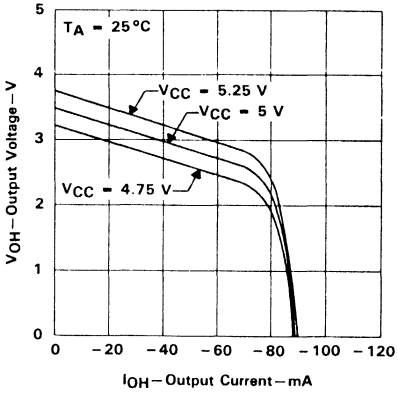


FIGURE 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

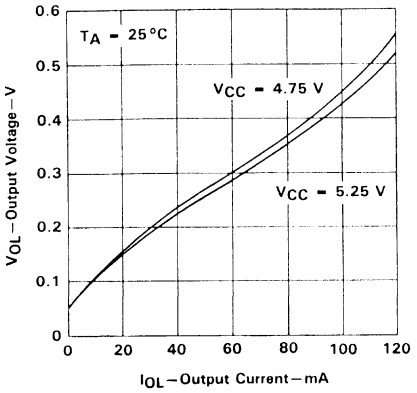


FIGURE 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

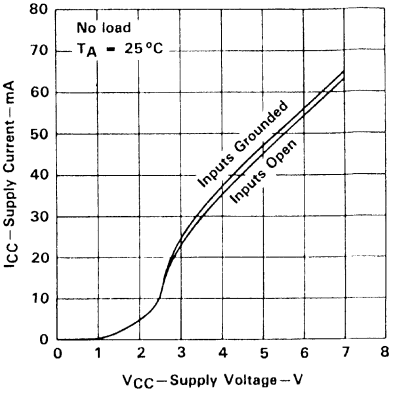


FIGURE 10

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

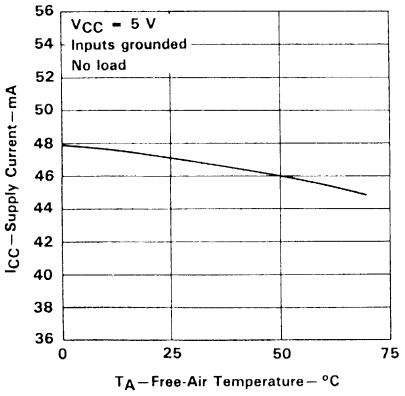


FIGURE 11

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

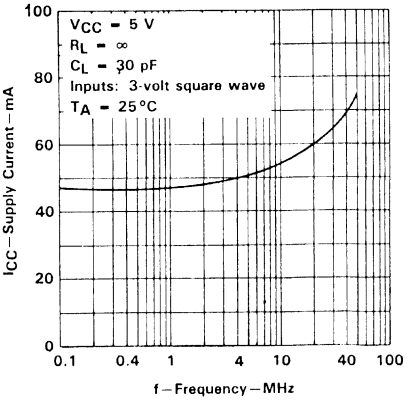


FIGURE 12

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

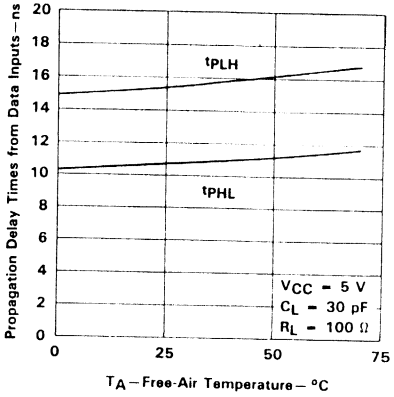


FIGURE 13

OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE

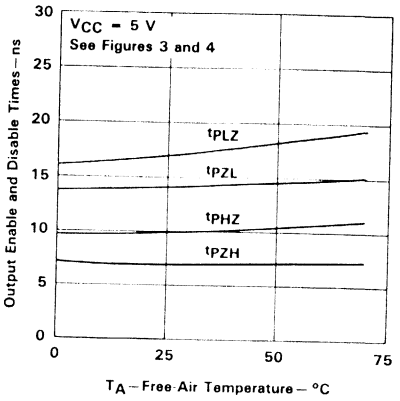


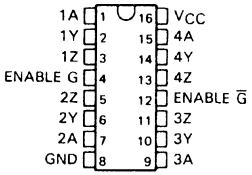
FIGURE 14

SN75172
QUADRUPLE DIFFERENTIAL LINE DRIVER

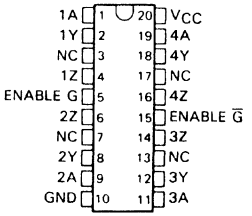
APRIL 1988

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of −7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable with AM26LS31**

J OR N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

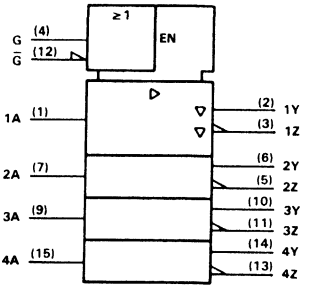
The SN75172 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS

logic symbol†



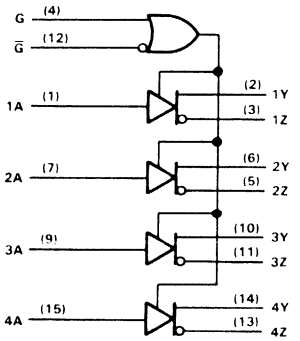
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

FUNCTION TABLE
(EACH DRIVER)

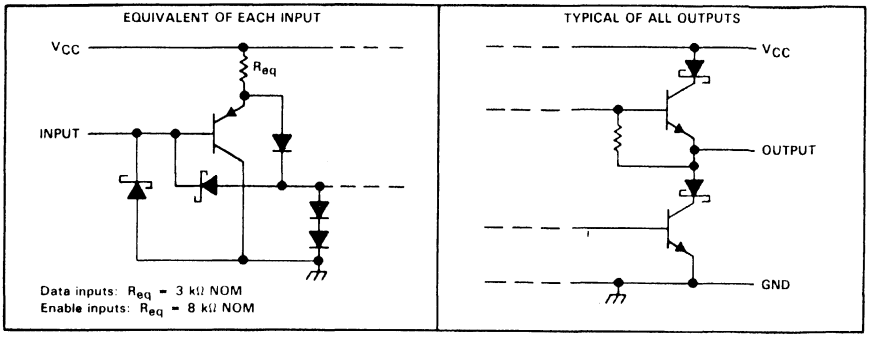
INPUT	ENABLES		OUTPUTS	
A	G	G̅	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			
				2			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage§					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}
NOTE 2: See EIA Standard RS-485 Figure 3-5, Test Termination Measurement 2.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V_t}\|\|$	$\|\|V_t\| - \|\overline{V_t}\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V_{os}}\|$	$\|V_{os} - \overline{V_{os}}\|$
I_{OS}	$\|I_{sa}\|, \|I_{sb}\|$	
I_O	$\|I_{xa}\|, \|I_{xb}\|$	I_{ia}, I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 2		45	65	ns
t_{TD}	Differential-output transition time			80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 4		18	30	ns

PARAMETER MEASUREMENT INFORMATION

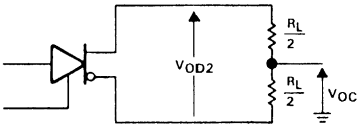


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

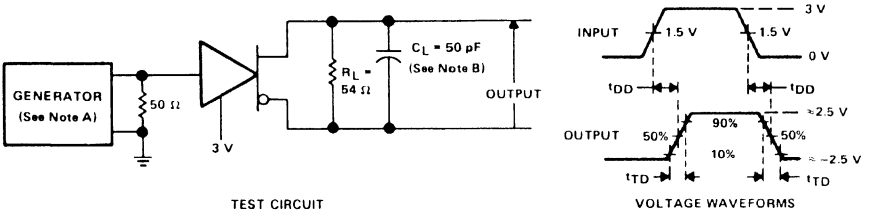


FIGURE 2. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

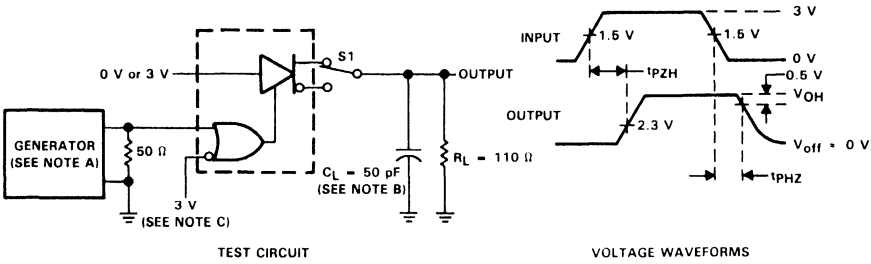


FIGURE 3. t_{PZH} AND t_{PHZ}

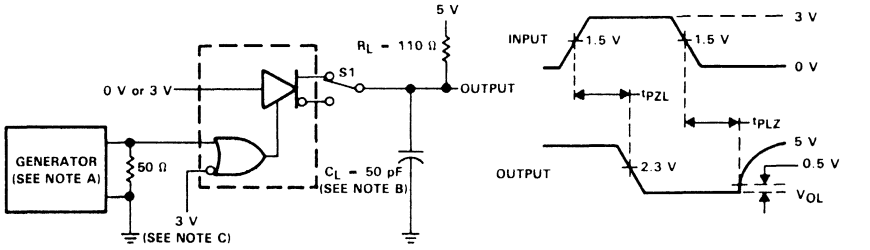


FIGURE 4. t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \leq 5$ ns, $t_f \leq 5$ ns, PRR $\leq$ 1 MHz, duty cycle = 50%, Z_{out} = 50 Ω.
B. C_L include probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

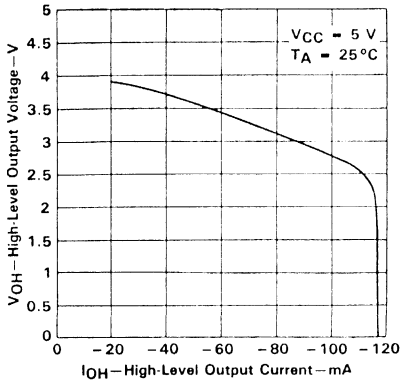


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

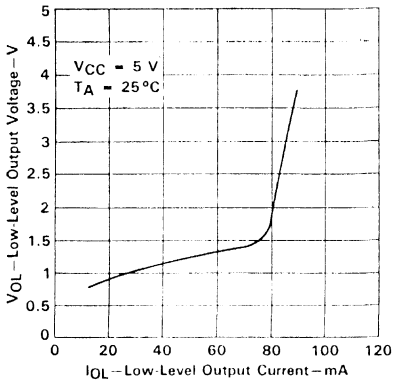


FIGURE 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

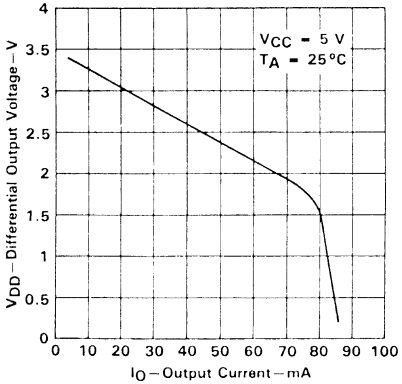


FIGURE 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

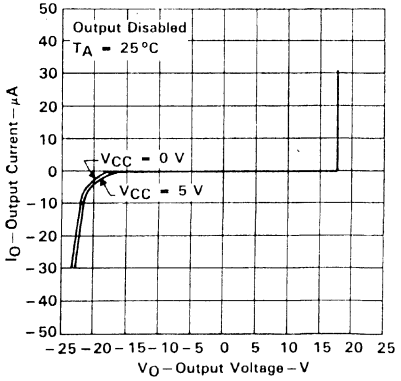


FIGURE 8

TYPICAL CHARACTERISTICS

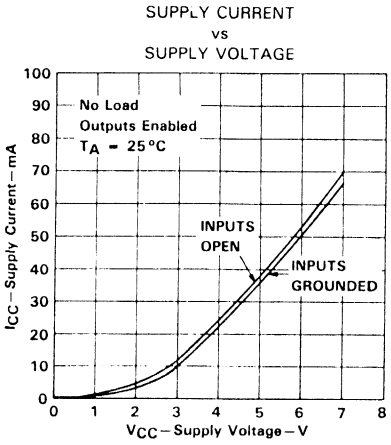


FIGURE 9

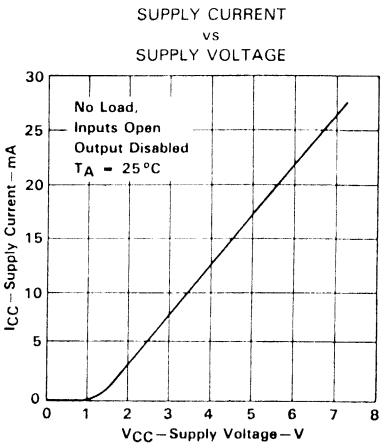
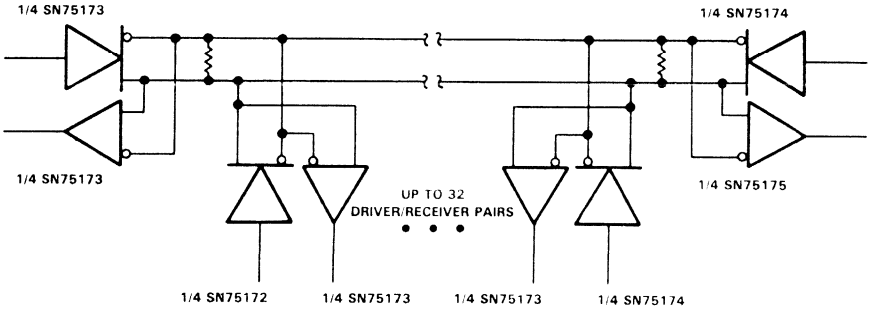


FIGURE 10

TYPICAL APPLICATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

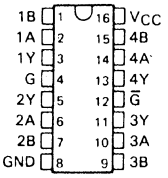
FIGURE 11

SN75173
QUADRUPLE DIFFERENTIAL LINE RECEIVER

JULY 1990

- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range . . . −12 to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Plug-In Replacement for AM26LS32**

D, J, OR N PACKAGE
(TOP VIEW)

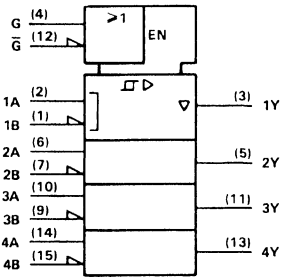


description

The SN75173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 to 12 V. Fail safe design ensures that if the inputs are open circuited, the outputs will always be high. The SN75173 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

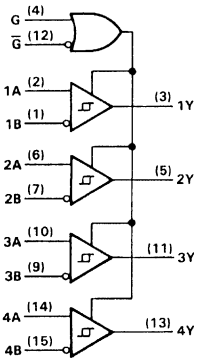
The SN75173 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



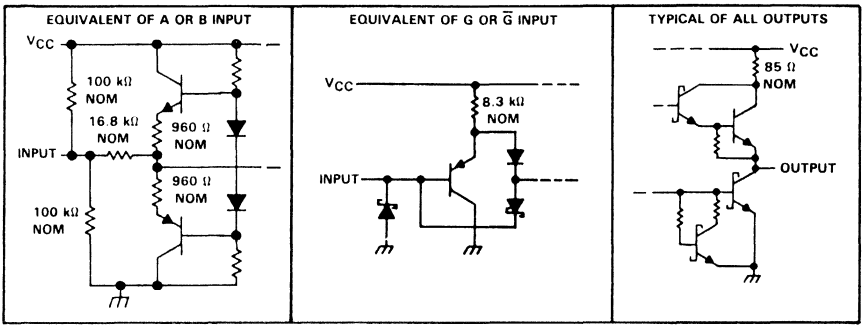
TEXAS INSTRUMENTS

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75173 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 4: Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF,			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

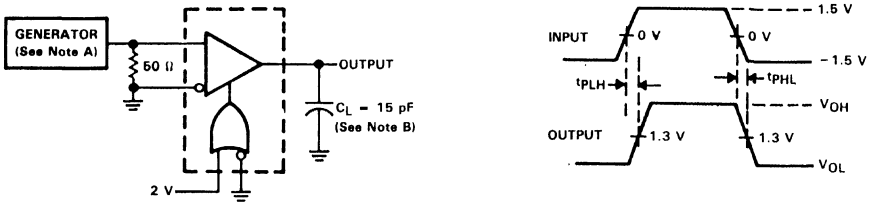


FIGURE 1. t_{PLH}, t_{PHL}

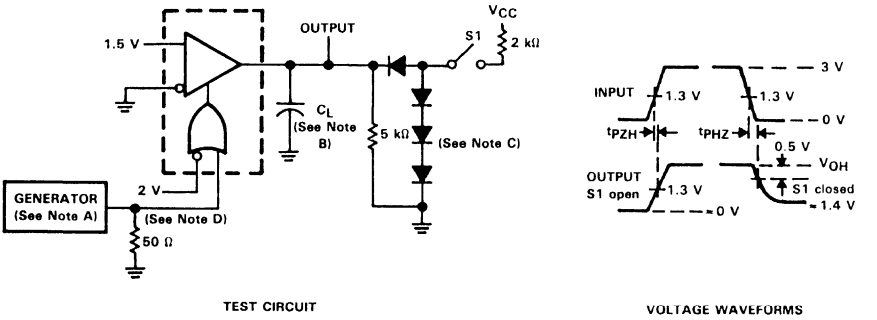


FIGURE 2. t_{PHZ}, t_{PZH}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

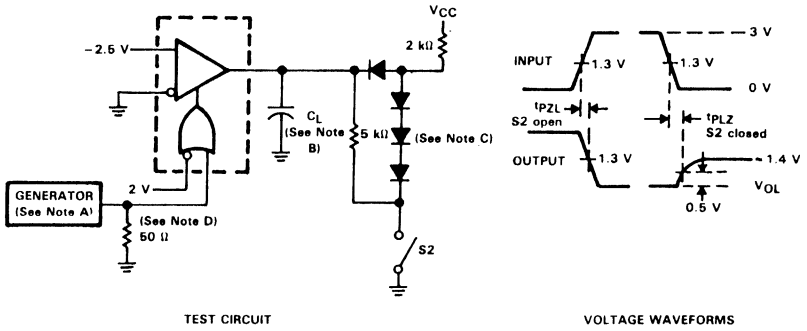


FIGURE 3. t_{PZL}, t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

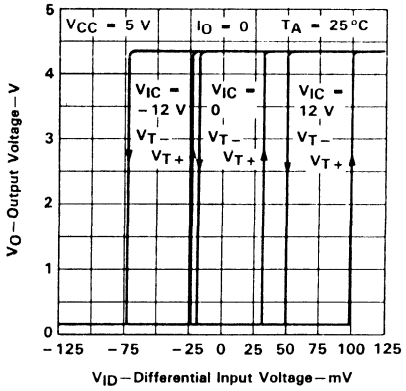


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

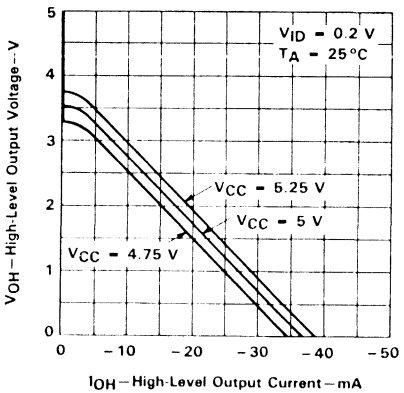


FIGURE 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

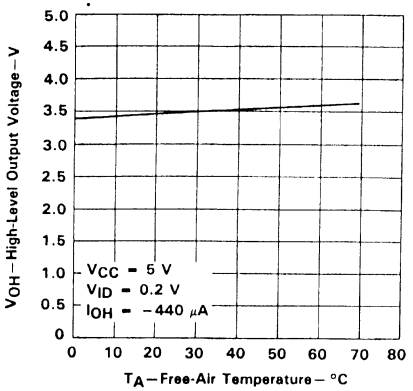


FIGURE 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

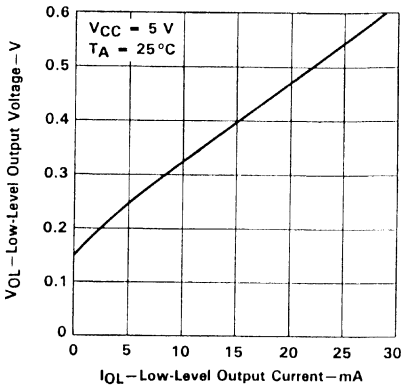


FIGURE 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

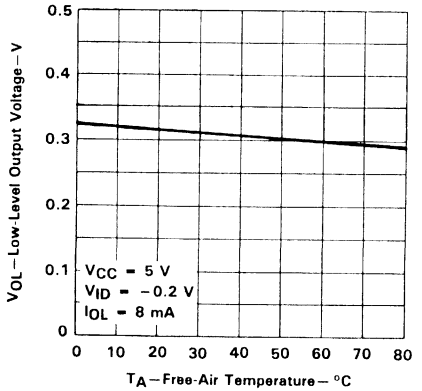


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

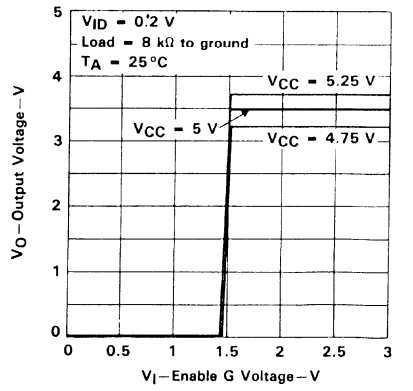


FIGURE 9

TYPICAL CHARACTERISTICS

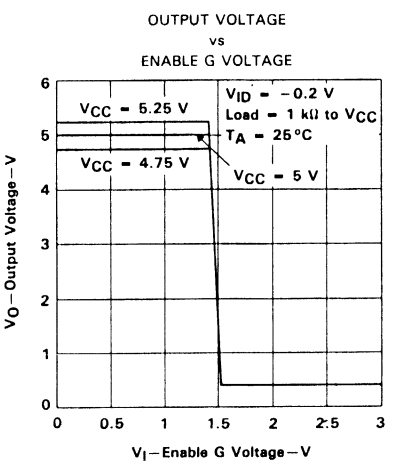


FIGURE 10

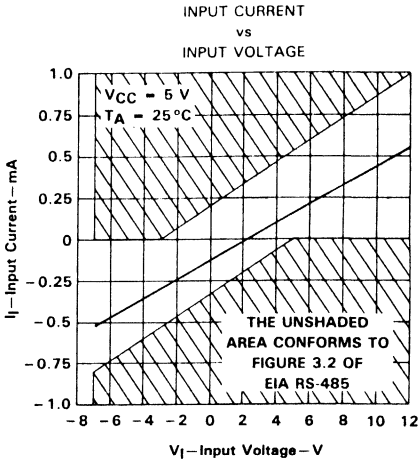
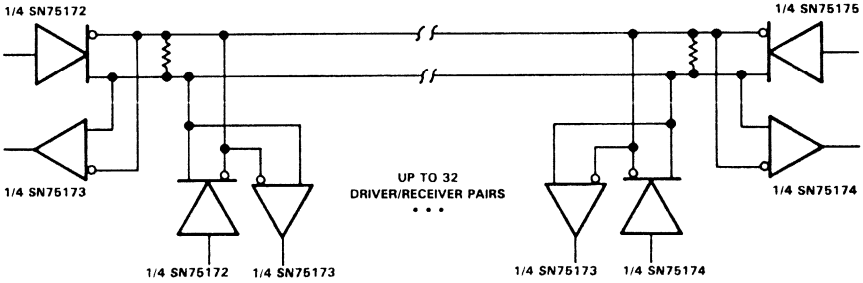


FIGURE 11

TYPICAL APPLICATION



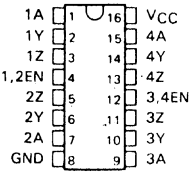
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

SN75174
QUADRUPLE DIFFERENTIAL LINE DRIVER

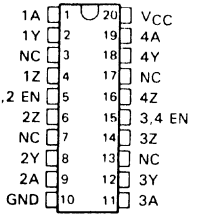
MAY 1988

- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of −7 V to 12 V**
- **Active-High Enable**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable with MC3487**

J OR N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN75174 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

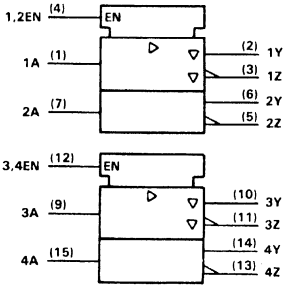
The SN75174 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, X = irrelevant,
L = TTL low level, Z = High impedance (off)

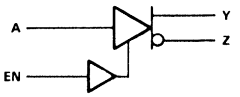
logic symbol†



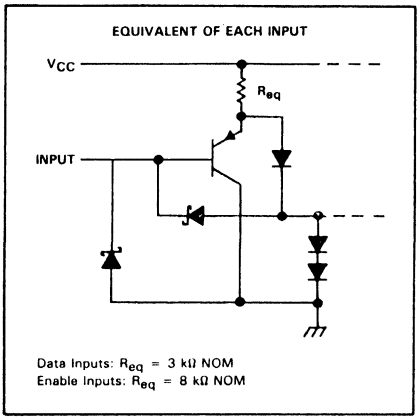
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

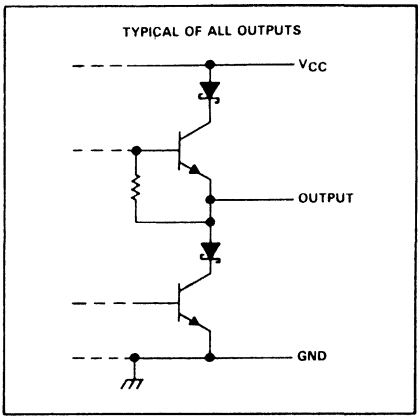
TEXAS INSTRUMENTS

logic diagram, each driver (positive logic)



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-Level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output curent, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	½ V_{OD1}			V
		R_L = 54 Ω,	See Figure 1	2			
				1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common mode output voltage					+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Oututs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 2: See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 2		45	65	ns
t_{TD}	Differential-output transition time			80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 4		55	80	ns
t_{PHZ}	Outut disable time from high level	R_L = 110 Ω, See Figure 3		75	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 4		18	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

PARAMETER MEASUREMENT INFORMATION

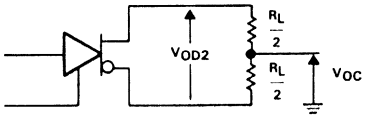
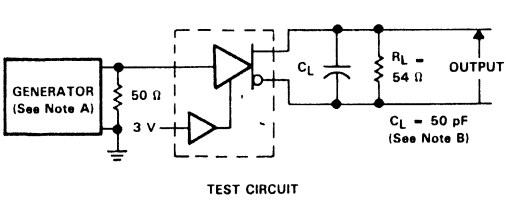
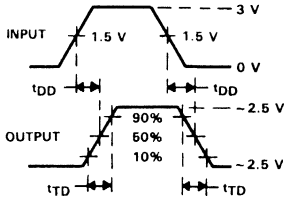


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT

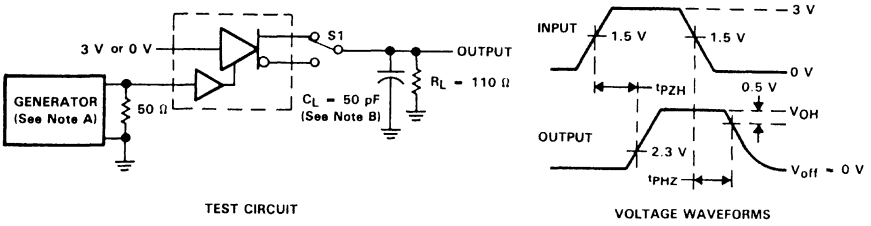


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

FIGURE 2. DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

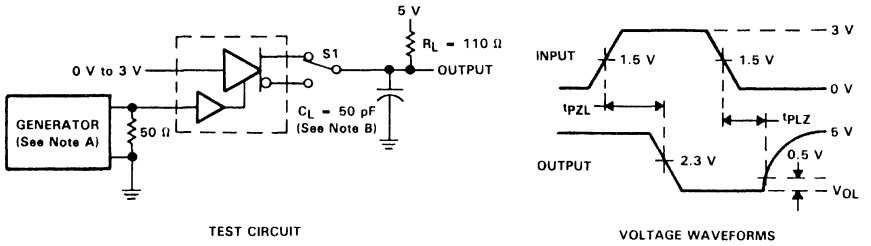
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 3. t_{PZH} AND t_{PHZ}



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 4. t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

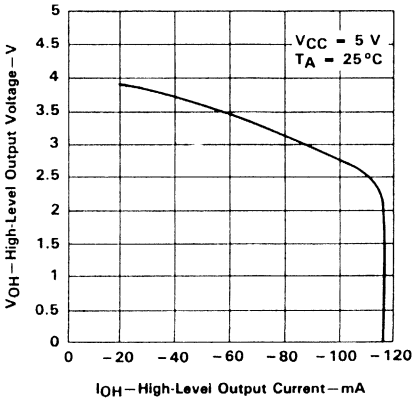


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

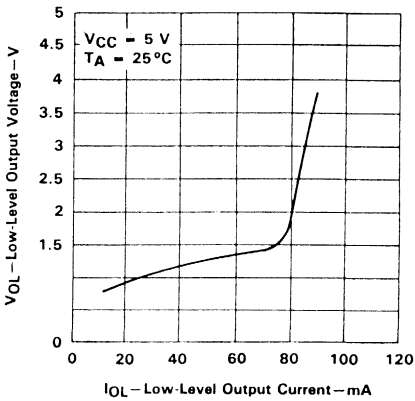


FIGURE 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

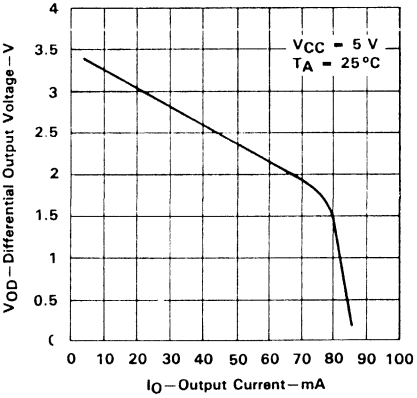


FIGURE 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

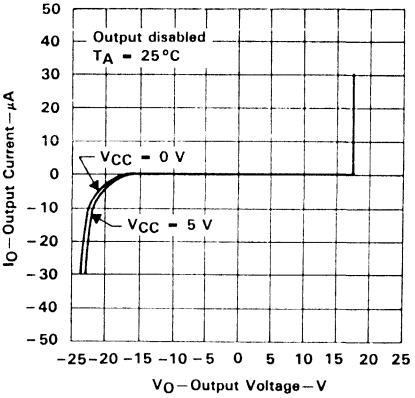


FIGURE 8

TYPICAL CHARACTERISTICS

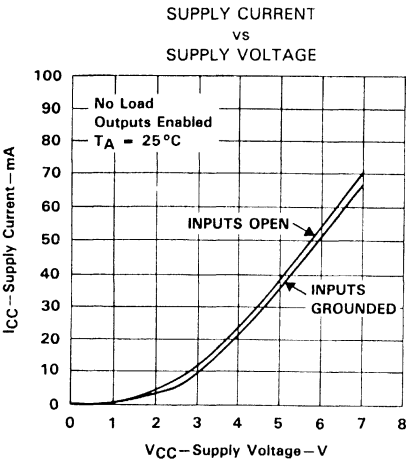


FIGURE 9

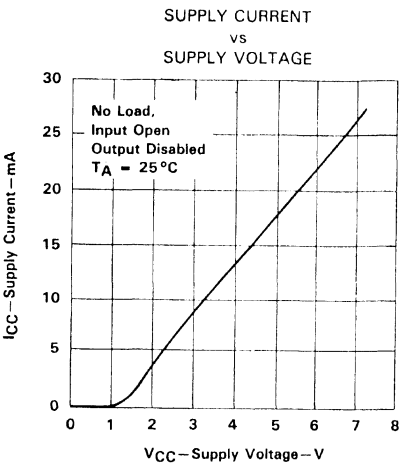
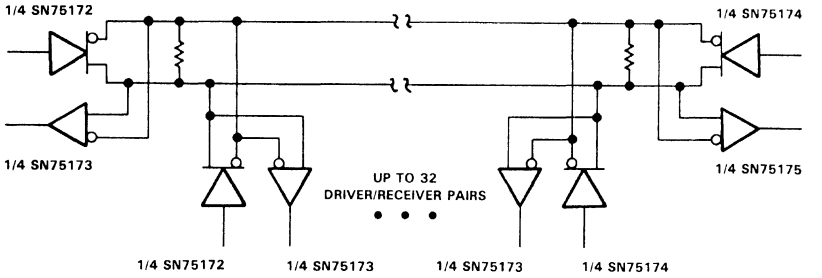


FIGURE 10

TYPICAL APPLICATION

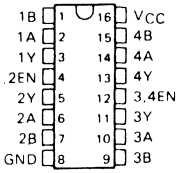


NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11

- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Plug-in Replacement for MC3486**

D, J, OR N PACKAGE
(TOP VIEW)



description

The SN75175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of ±12 V. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

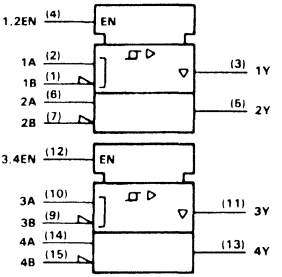
The SN75175 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} <$ 0.2 V	H	?
$V_{ID} \geq -0.2$ V	H	L
X	L	Z

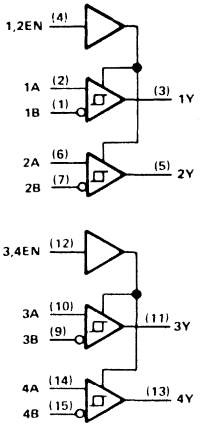
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

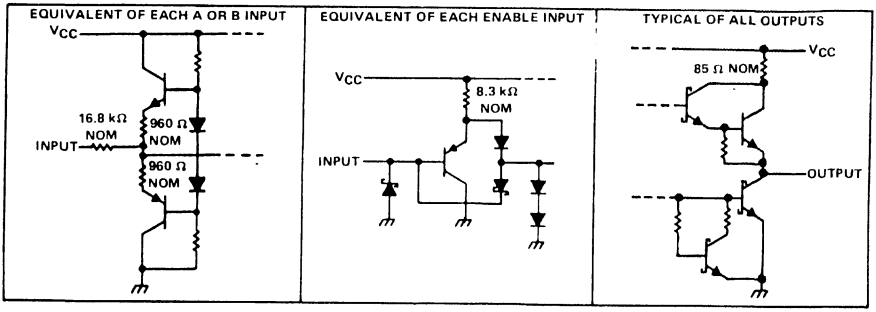


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . −300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . −260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75175 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level enable input voltage, V_{IH}	2			V
Low level enable input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 16 mA		−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less postitive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 4: Refer to EIA standards RS-422-A, RS-423-A, and RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level			25	35	ns

PARAMETER MEASUREMENT INFORMATION

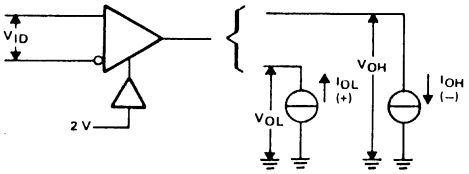
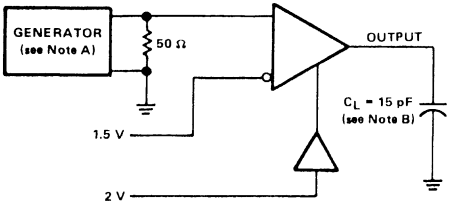
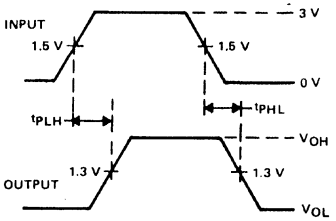


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

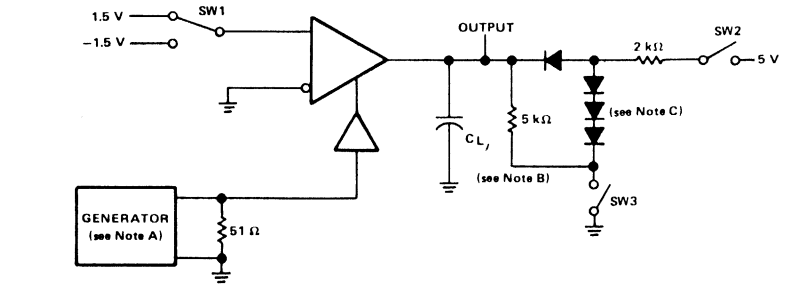


VOLTAGE WAVEFORMS

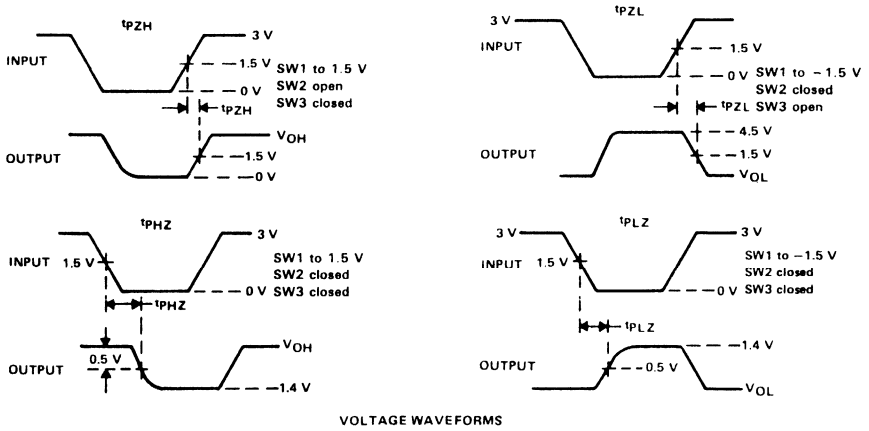
FIGURE 2. PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_f \leq 6$ ns, $t_r \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

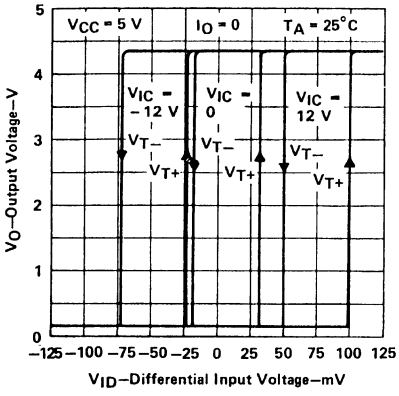


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

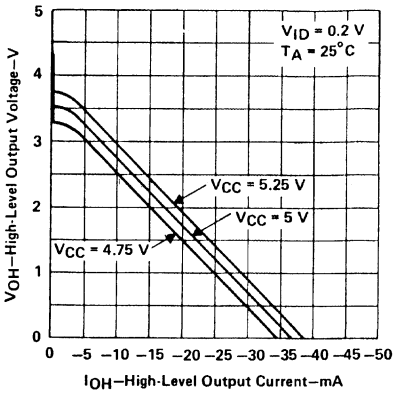


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

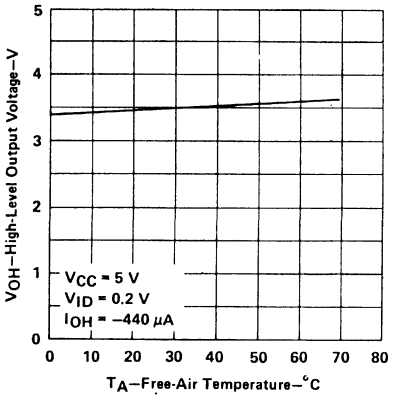


FIGURE 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

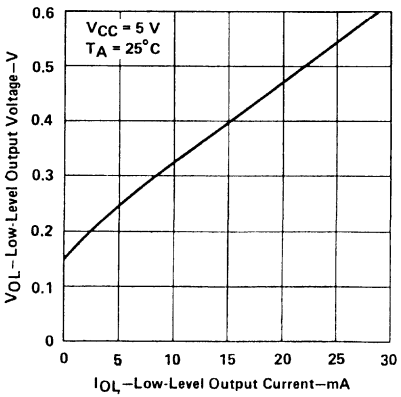


FIGURE 7

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

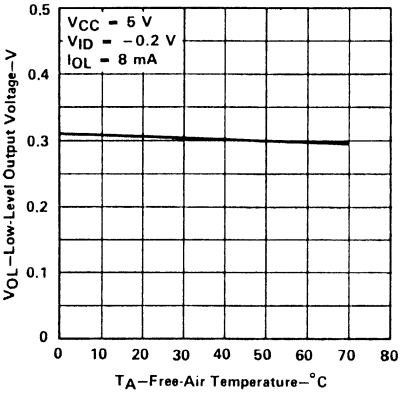


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

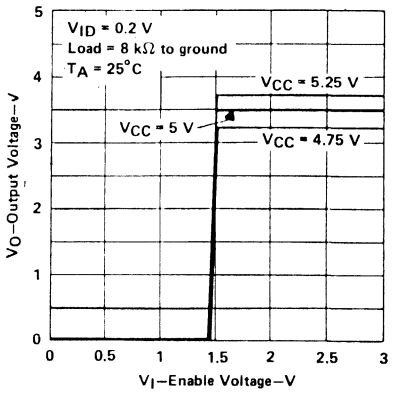


FIGURE 9

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

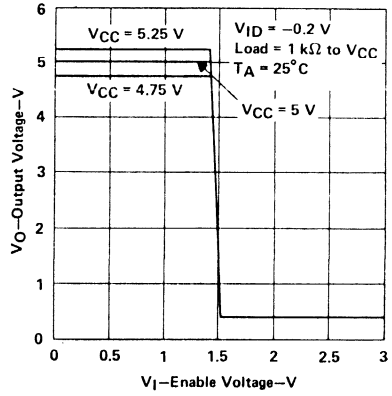


FIGURE 10

SUPPLY CURRENT
(ALL RECEIVERS)
vs
SUPPLY VOLTAGE

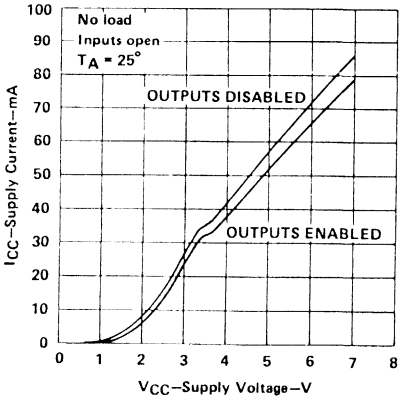


FIGURE 11

TYPICAL CHARACTERISTICS

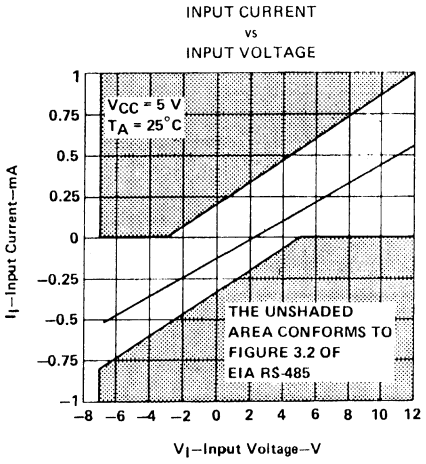


FIGURE 12

TYPICAL APPLICATION

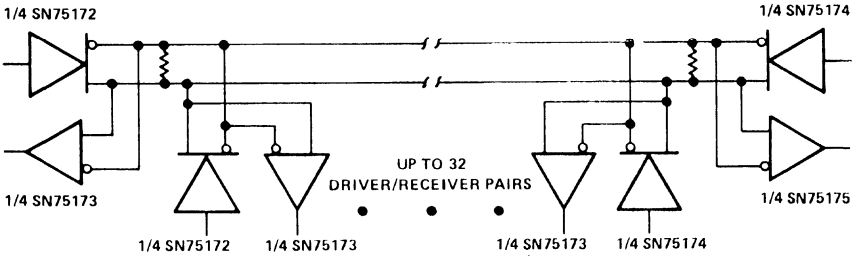
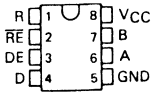


FIGURE 13

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

- Bidirectional Transceiver
- Meets EIA Standards RS-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

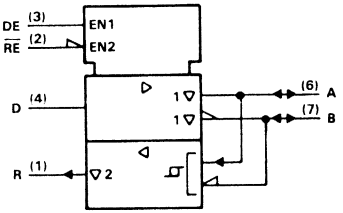
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

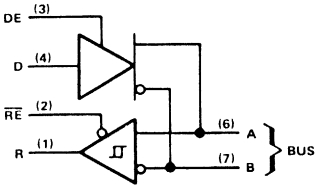
The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27.

The SN75176A combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

logic symbol



logic diagram (positive logic)

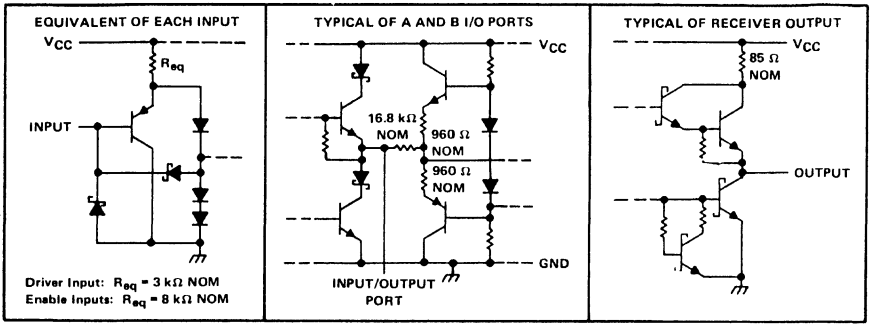


description (continued)

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and the SN75173 and SN75175 quadruple differential line receivers.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 725 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C and derate the P package to 640 mW at 70°C at the rate of 8.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0				2 V_{OD2}	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2	2.7		V
		R_L = 54 Ω,	See Figure 1	1.5	2.4		
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡					±0.2	V
V_{OC}	Common-mode output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 3		40	60	ns
t_{TD}	Differential-output transition time				65	95	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		55	90	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		85	130	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	40	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	30	ns
t_{PZL}	Output enable time to low level				12	30	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level				17	35	ns

PARAMETER MEASUREMENT INFORMATION

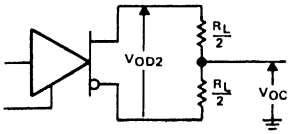


FIGURE 1. DRIVER V_{OD} AND V_{OC}

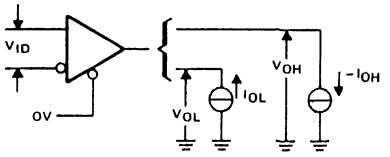
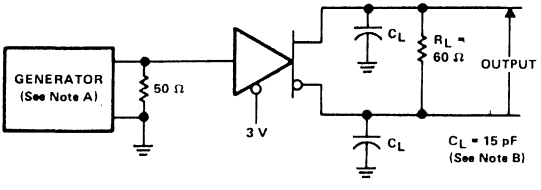
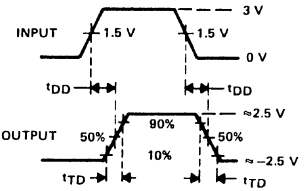


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

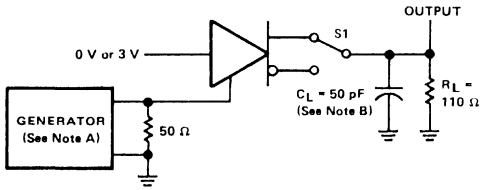


TEST CIRCUIT

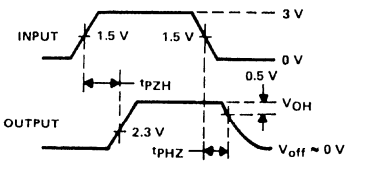


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

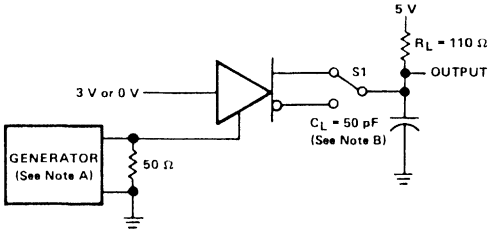


TEST CIRCUIT

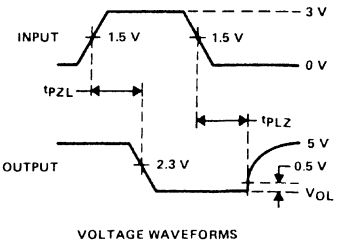


VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

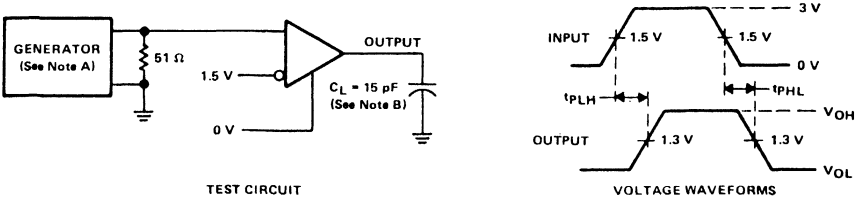


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

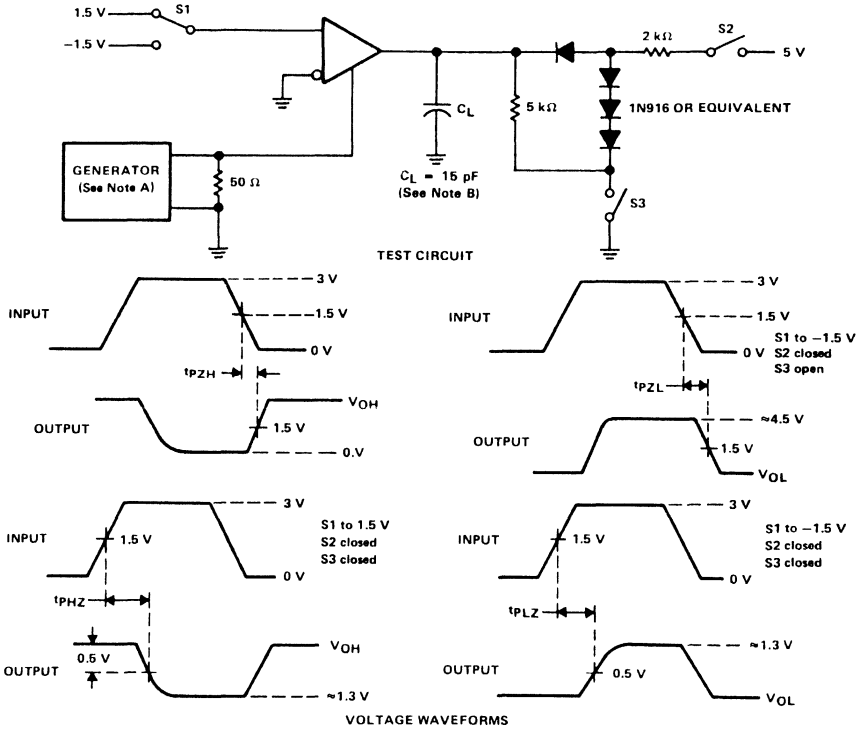


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

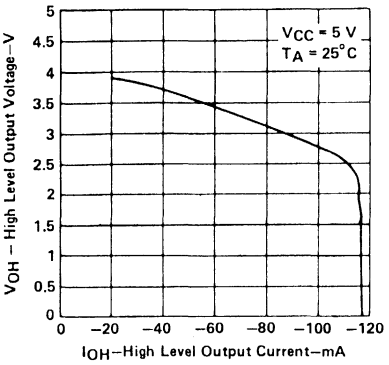


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

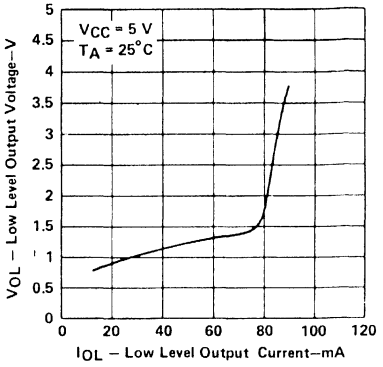


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

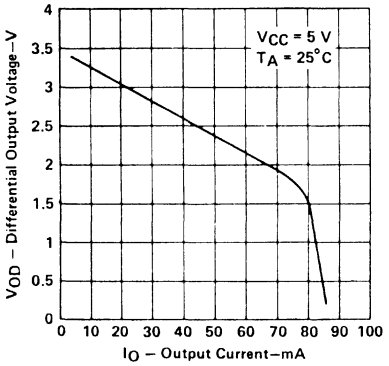


FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

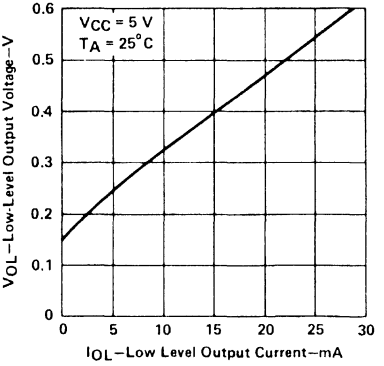


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

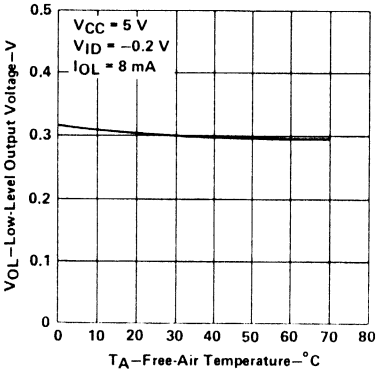


FIGURE 12

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

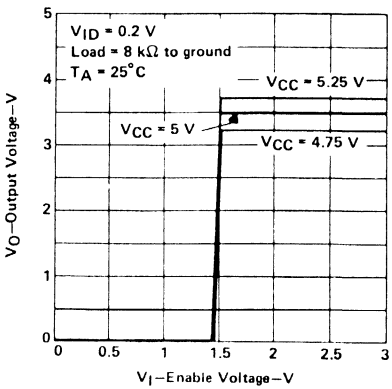


FIGURE 13

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

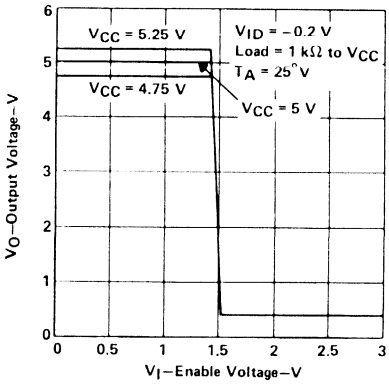
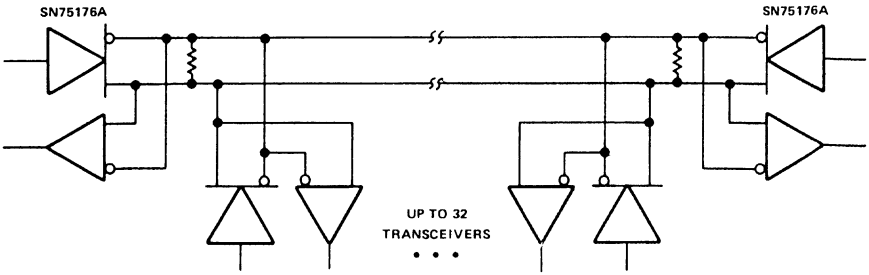


FIGURE 14.

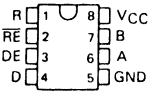
TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D, JG, OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} <$ 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

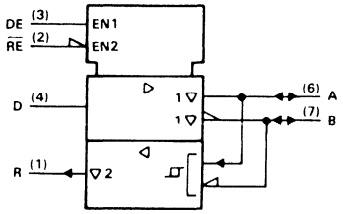
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27.

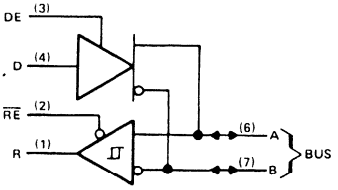
The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

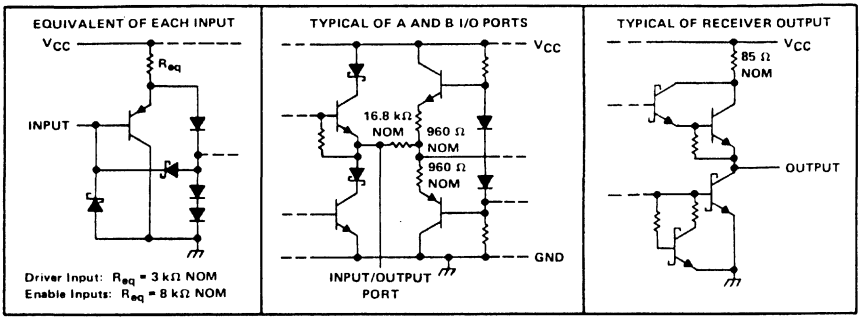


The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from −40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65176B . . . . . −40°C to 105°C
SN75176B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. In the JG package, the chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 105°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
JG	825 mW	6.6 mW/°C	528 mW	297 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

			MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12	V
					−7	
High-level input voltage, V_{IH}		D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}		D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)					±12	V
High-level output current, I_{OH}		Driver			−60	mA
		Receiver			−400	μA
Low-level output current, I_{OL}		Driver			60	mA
		Receiver			8	
Operating free-air temperature, T_A	SN65176B		−40		105	°C
	SN75176B		0		70	

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			
				2			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω, See Figure 1				+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
I_O	Output current	Output disabled, See Note 5	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 4. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
5. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3			15	22	ns
t_{TD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4			85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5			40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4			150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5			20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, I_{OH} = −400 μA, See Figure 2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 6	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 6: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V, C_L = 15 pF, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

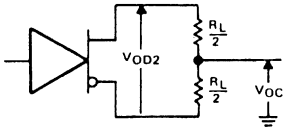


FIGURE 1. DRIVER V_{OD} AND V_{OC}

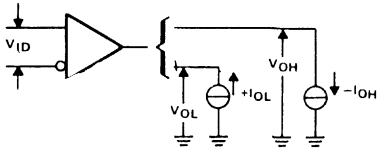


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

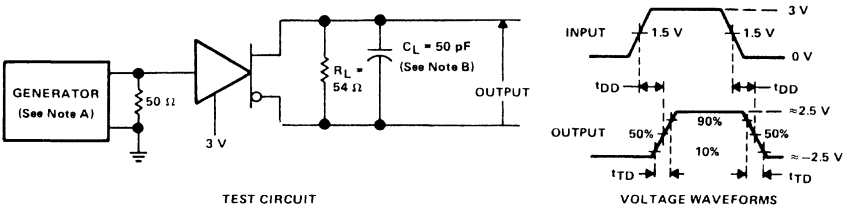


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

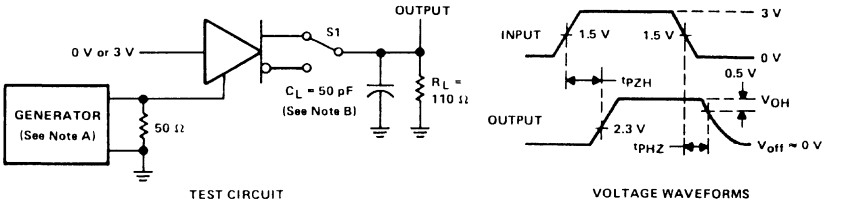


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

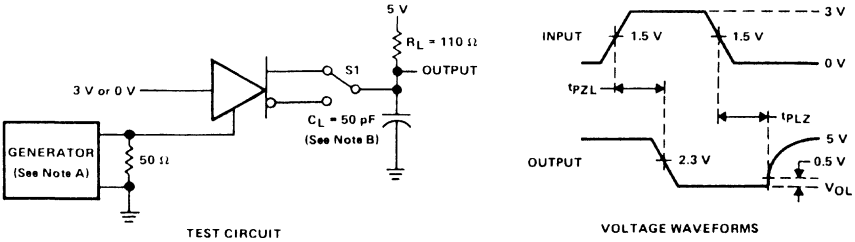
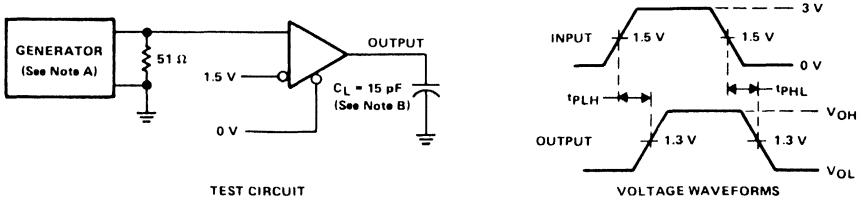


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

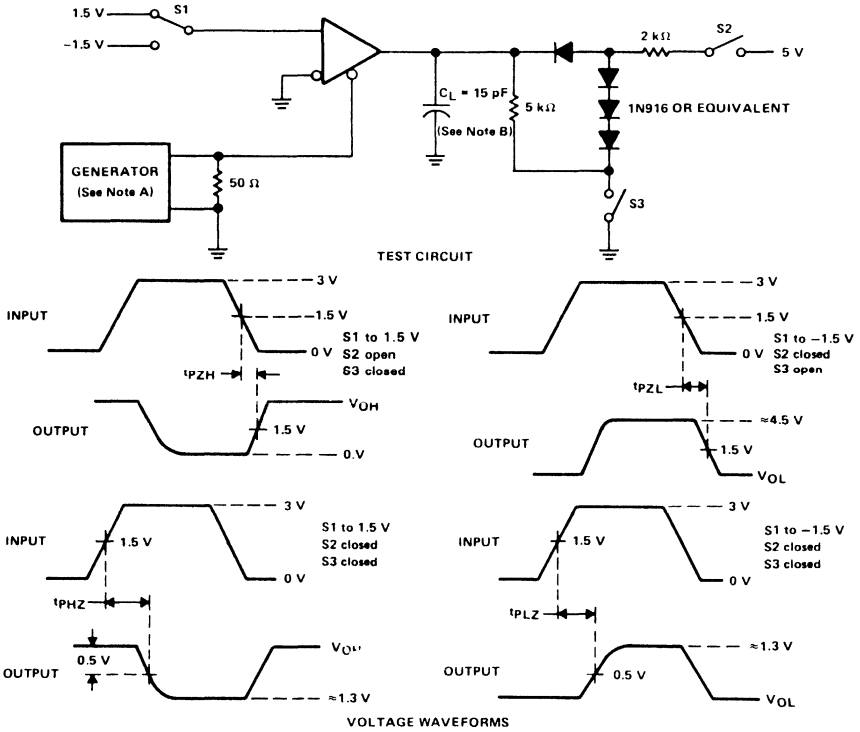
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 6. RECEIVER PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS

FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

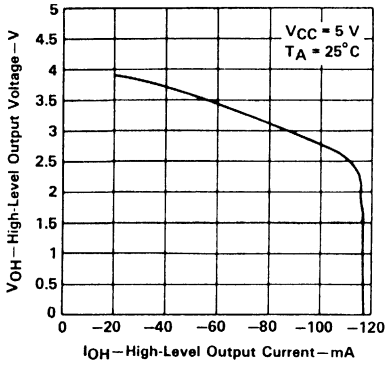


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

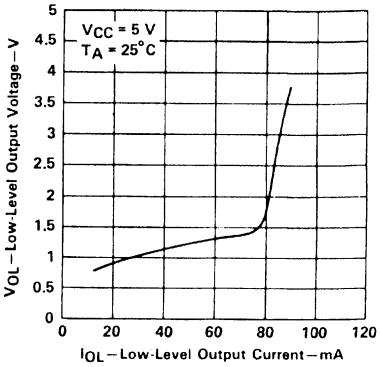


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

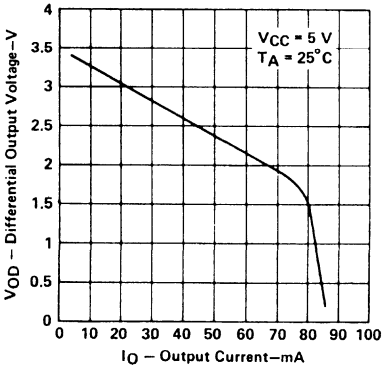


FIGURE 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

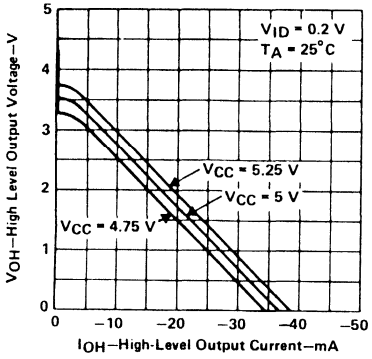


FIGURE 11

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

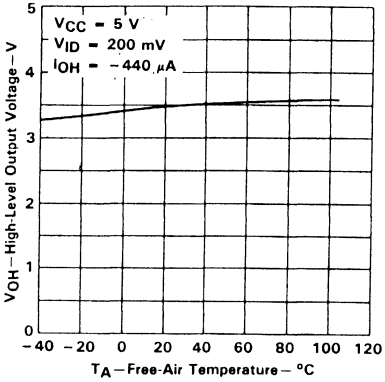


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

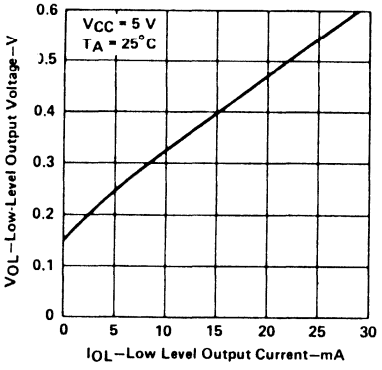


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

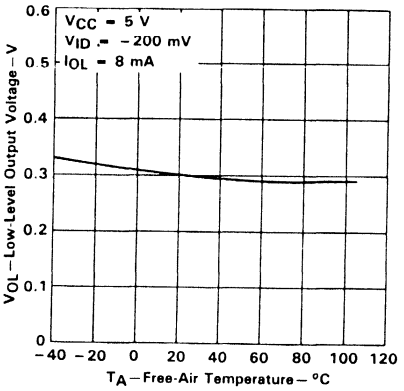


FIGURE 14

TYPICAL CHARACTERISTICS

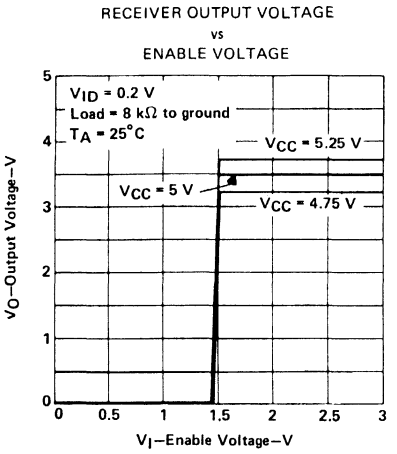


FIGURE 15

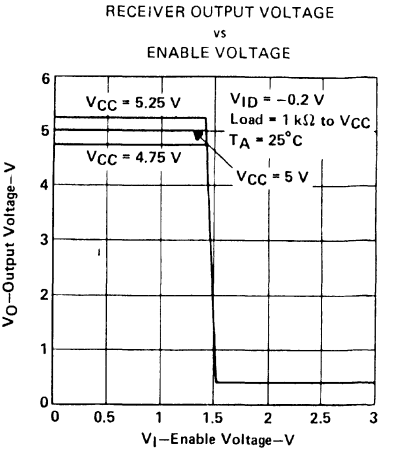


FIGURE 16

TYPICAL APPLICATION

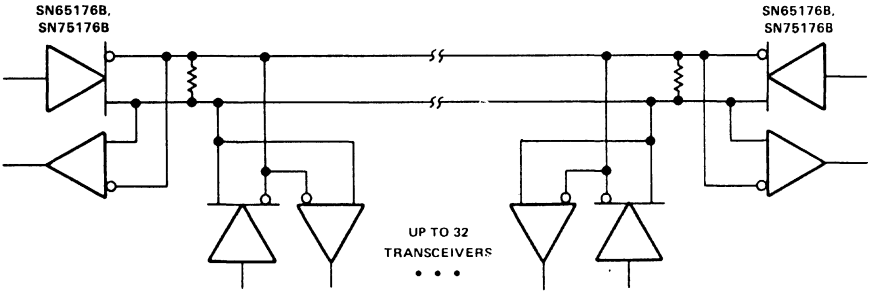


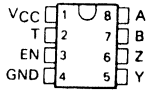
FIGURE 17. TYPICAL APPLICATION CIRCUIT

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

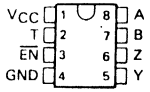
TEXAS INSTRUMENTS

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

SN75177B . . . D, JG, OR P PACKAGE
(TOP VIEW)



SN75178B . . . JG OR P PACKAGE
(TOP VIEW)



SN75177B FUNCTION TABLE

DIFFERENTIAL INPUTS A−B	ENABLE EN	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq 0.2$ V	H	L	L	H
X	L	Z	Z	Z

SN75178B FUNCTION TABLE

DIFFERENTIAL INPUTS A−B	ENABLE $\overline{EN}$	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq 0.2$ V	L	L	L	H
X	H	Z	Z	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = impedance (off)

description

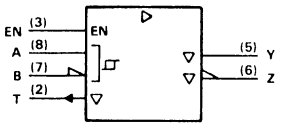
The SN75177B and SN75178B differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177B and SN75178B are identical except for the complementary enable inputs, which allow the devices to be used in pairs for bidirectional communication.

The SN75177B and SN75178B feature positive- and negative-current limiting 3-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −7 V to 12 V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The driver is designed to drive current loads up to 60 mA maximum.

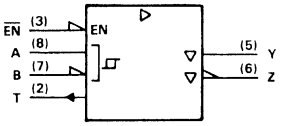
The SN75177B and SN75178B are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176B bus transceiver.

logic symbols†

SN75177B



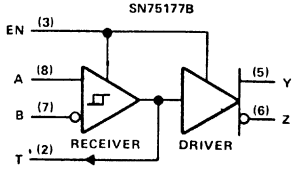
SN75178B



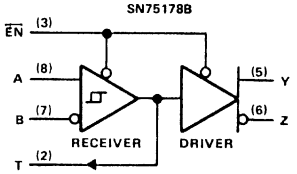
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

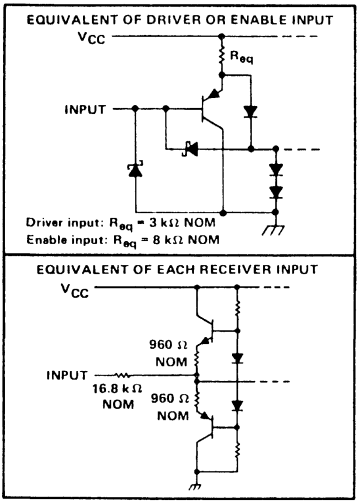
SN75177B

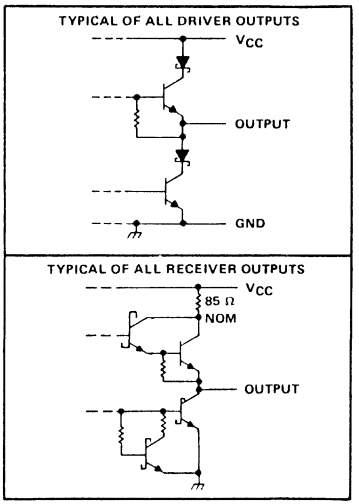


SN75178B



schematics of inputs and outputs





TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75177B and SN75178B chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	EN or $\overline{EN}$	2			V
Low-level input voltage, V_{IL}	EN or $\overline{EN}$			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		$\frac{1}{2}V_{OD1}$			V
				2			
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-stage output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 4: See EIA Standard RS-485 from Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3		15	22	ns
t_{TD}	Differential-output transition time			20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				20	μA
						−400	
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−200	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 12.
NOTE 5: Refer to EIA Standard RS-422 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		30	40	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 8		25	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

PARAMETER MEASUREMENT INFORMATION

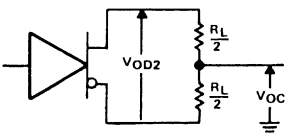


FIGURE 1. DRIVER V_{OD} AND V_{OC}

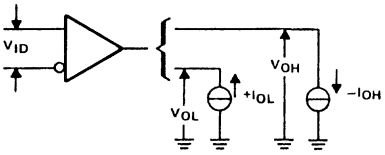


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

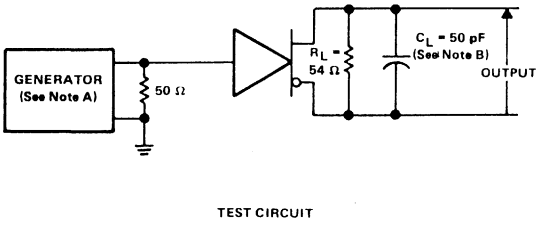


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

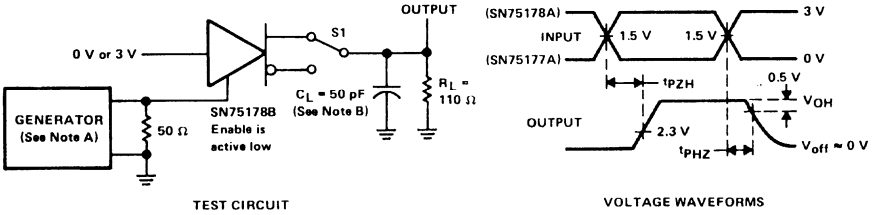
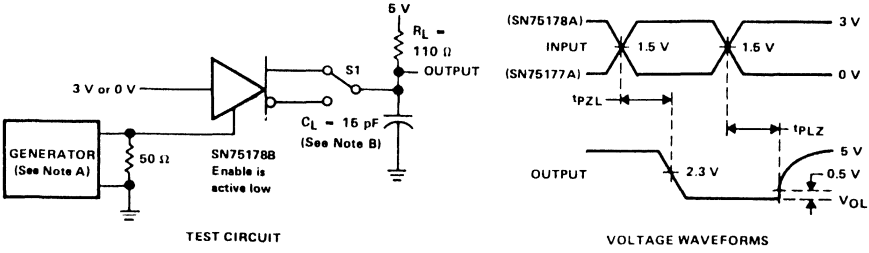


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES (t_{PZH}, t_{PHZ})

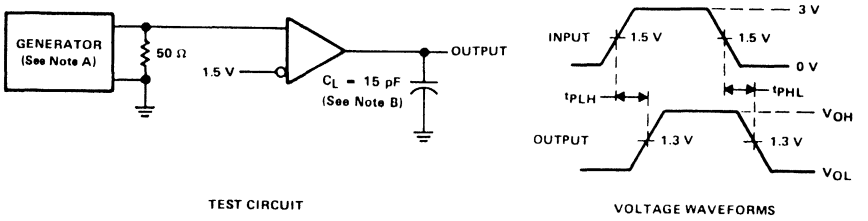
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES (t_{PZL}, t_{PLZ})

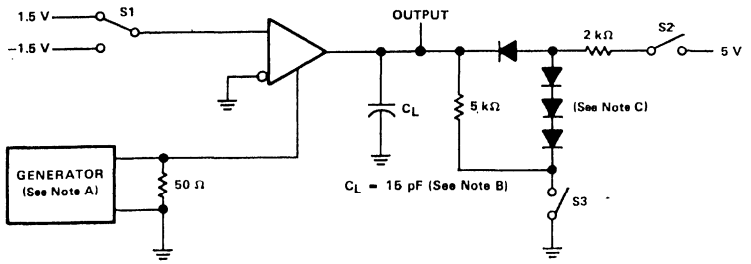


TEST CIRCUIT VOLTAGE WAVEFORMS

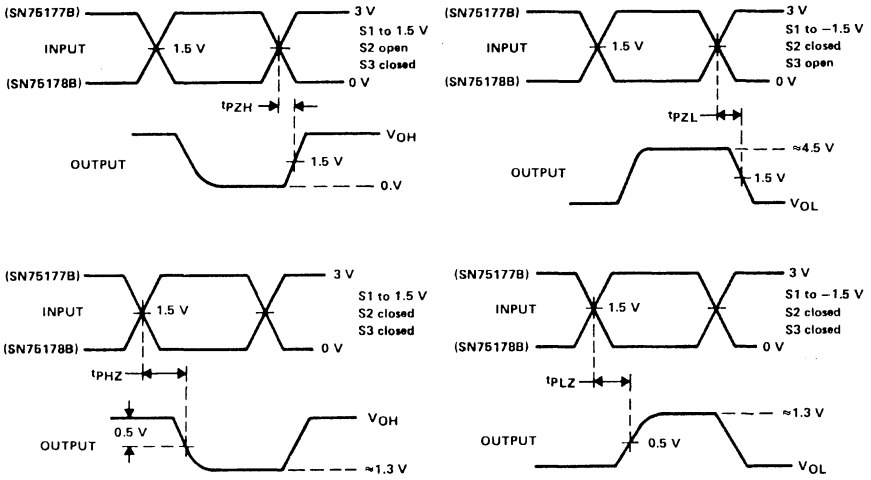
FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns, $Z_0 = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 7. RECEIVER ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

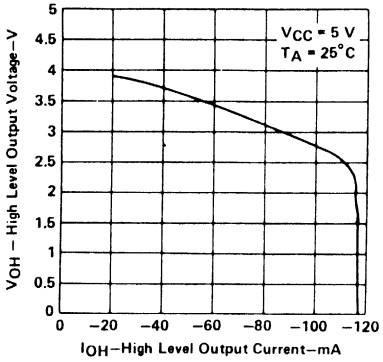


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

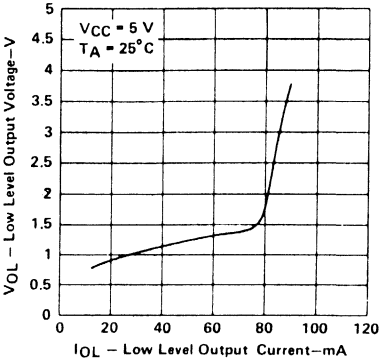


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

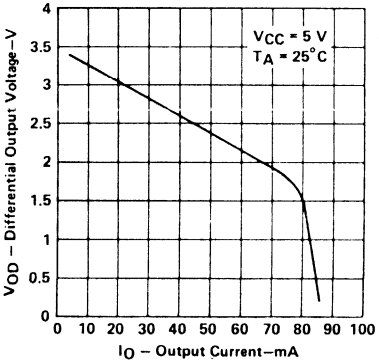


FIGURE 10

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

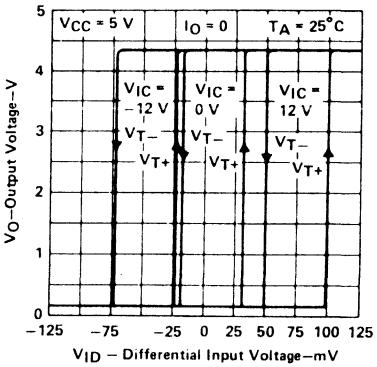


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

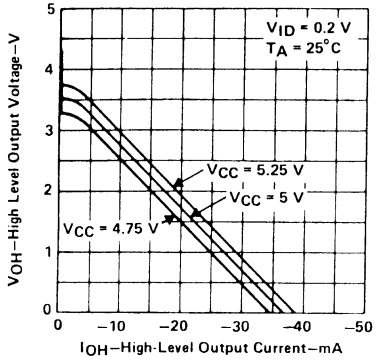


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

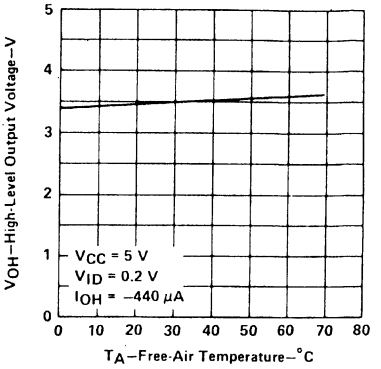


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

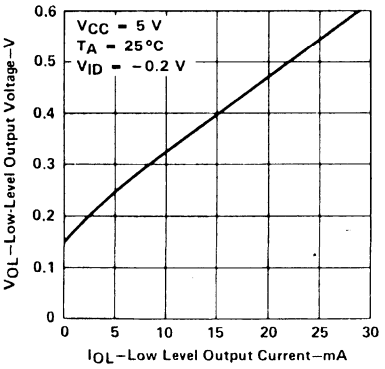


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

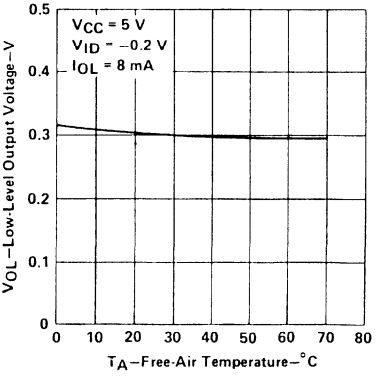
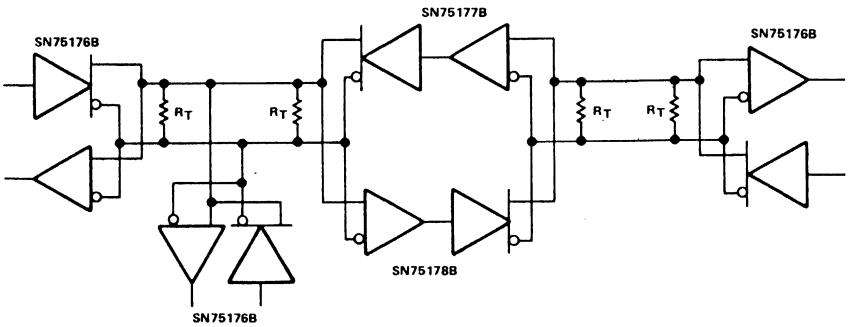


FIGURE 15

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

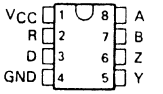
FIGURE 16. TYPICAL APPLICATION CIRCUIT

SN75179B
DIFFERENTIAL DRIVER AND LINE RECEIVER PAIR

AUGUST 1989

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D, JG, OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	OUTPUTS
D	Y Z
H	H L
L	L H

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	OUTPUT
A − B	R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

H = high level, L = low level, ? = indeterminate

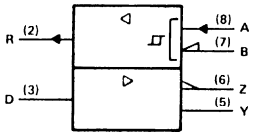
description

The SN75179B driver and bus receiver circuit is a monolithic integrated device designed for balanced transmission line applications and meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver outputs provide limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The device is designed to drive current loads of up to 60 mA maximum.

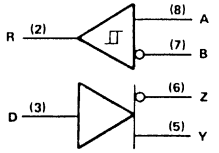
The SN75179B is characterized for operation from 0°C to 70°C.

logic symbol†

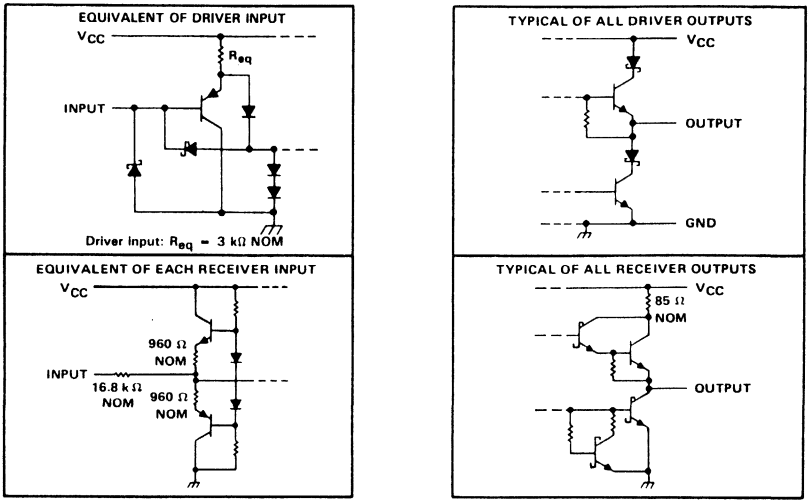


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage at any bus terminal	−10 V to 15 V
Differential input voltage (see Note 2)	±25 V
Continuous total dissipation at (or below 25°C free-air temperature (see Note 3):	
D package	725 mW
JG package	825 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C , the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C.. In the JG package SN75179B, chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	$\frac{1}{2}V_{OD1}$			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
$\lvert V_{OD3}\rvert$	Differential output voltage	See Note 4		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§					±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC} or 12 V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 4: See EIA Standard RS-485, Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{TD}	Differential-output transition time				20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
r_i	Input resistance			12			kΩ
i_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load			57	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 5: Refer to EIA Standard RS-422-A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 4		30	40	ns

PARAMETER MEASUREMENT INFORMATION

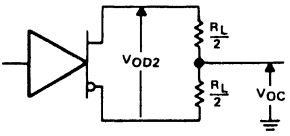


FIGURE 1. DRIVER V_{OD} AND V_{OC}

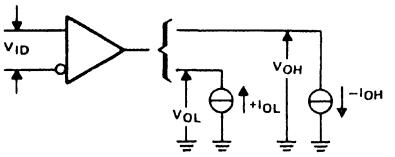
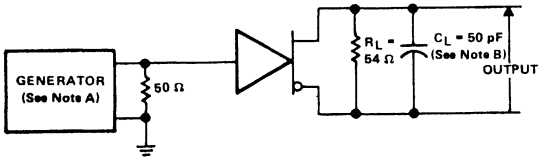
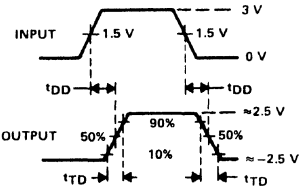


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

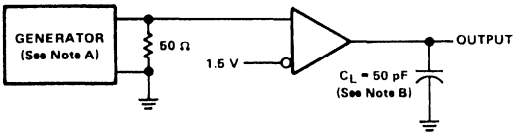


TEST CIRCUIT

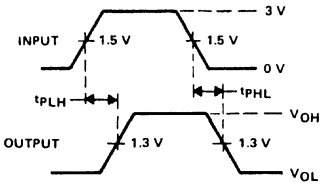


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

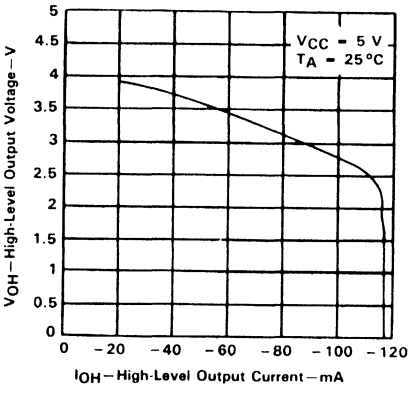


FIGURE 5

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

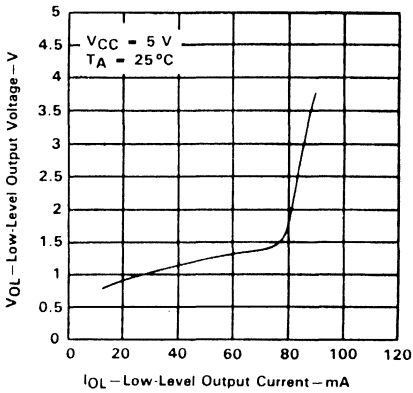


FIGURE 6

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

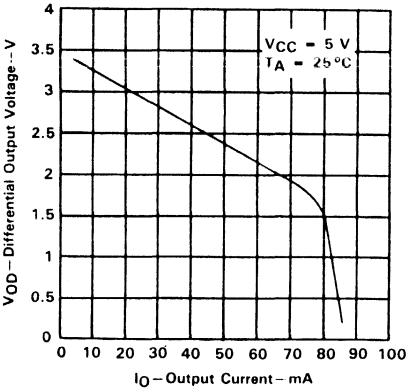


FIGURE 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

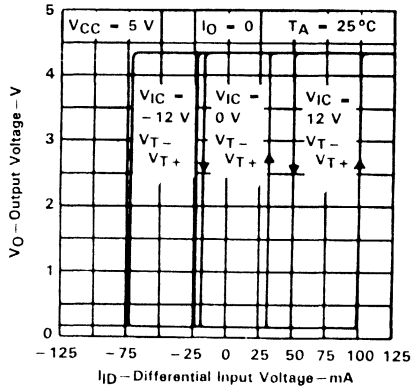


FIGURE 8

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

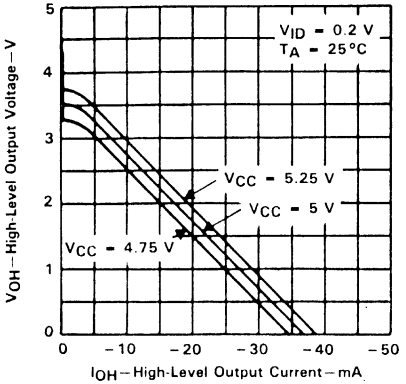


FIGURE 9

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

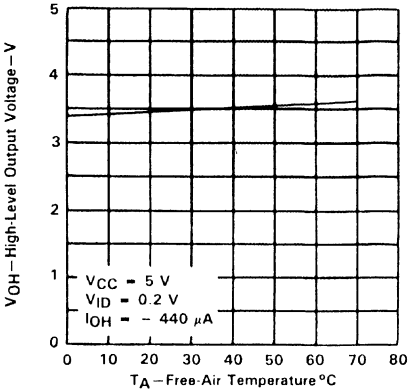


FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

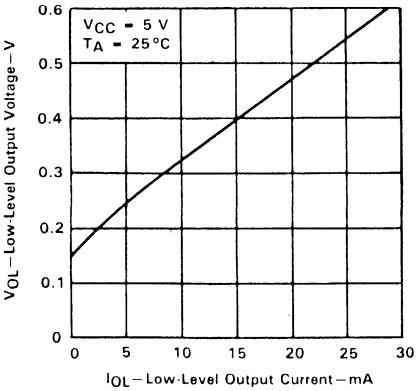


FIGURE 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

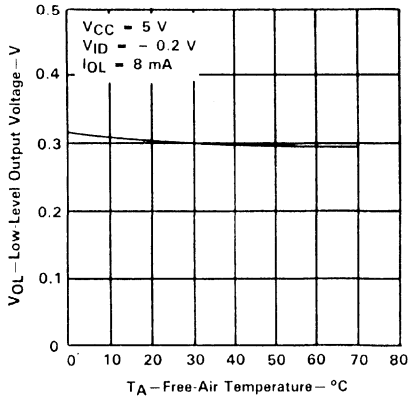
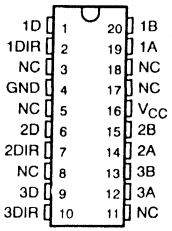


FIGURE 12

TEXAS INSTRUMENTS

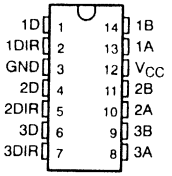
- Three Bidirectional Transceivers
- Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 90 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ± 60mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Features Independent Direction Controls for Each Channel

DW PACKAGE
(TOP VIEW)



NC–No internal connection

J PACKAGE
(TOP VIEW)



Function Table
(each driver)

INPUT D	DIR	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

Function Table
(each receiver)

DIFFERENTIAL INPUTS A – B	DIR	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
$-0.3\text{ V} < V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

description

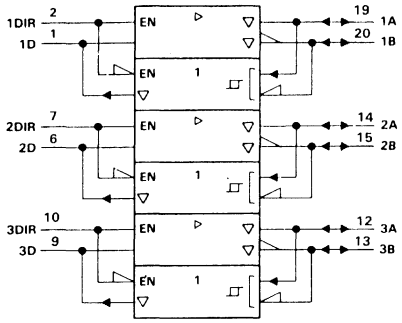
The SN75ALS170 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

description (continued)

The SN75ALS170 operates from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

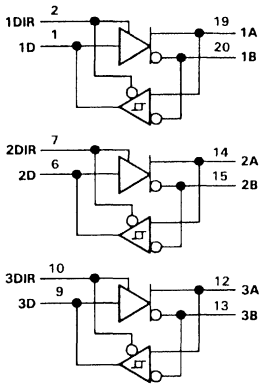
The SN75ALS170 is characterized for operation from 0°C to 70°C.

logic symbol†

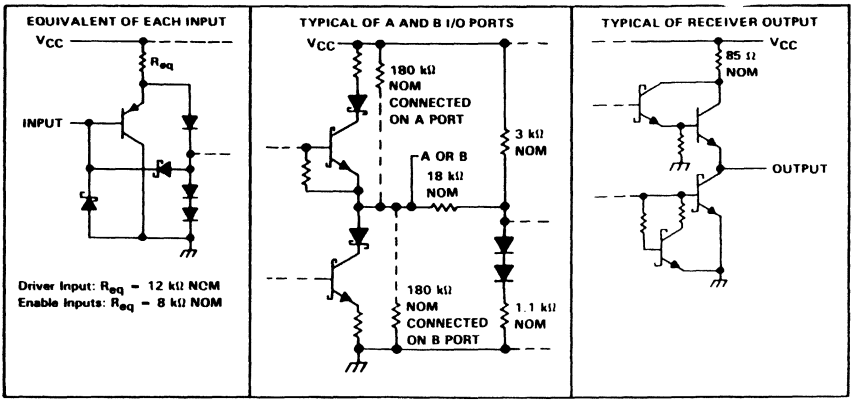


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12 −7	V
High-level input voltage, V_{IH}	D, DIR	2			V
Low-level input voltage, V_{IL}	D, DIR			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current¶	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short-circuit current should not exceed one second.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6	3	8	13	
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)	R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	6	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6		1	6	
t_{TD}	Differential-output transition time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6	3	8	13	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		30	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4	3	8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5	3	8	13	ns
t_{PDE}	Differential-output enable time	R_{L1} = R_{L3} = 165 Ω,	R_{L2} = 75 Ω,	8	30	45	ns
t_{PDZ}	Differential-output disable time	C_L = 60 pF,	See Figure 7	5	10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert V_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert V_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \bar{V}_{os} \rvert$	$\lvert V_{os} - \bar{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 8	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 8	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 2.4 V				20	µA
		V_O = 0.4 V				−400	
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 9	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

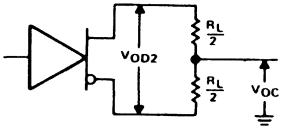


FIGURE 1. DRIVER V_{OD} AND V_{OC}

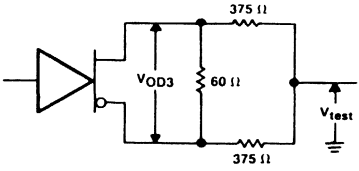


FIGURE 2. DRIVER V_{OD3}

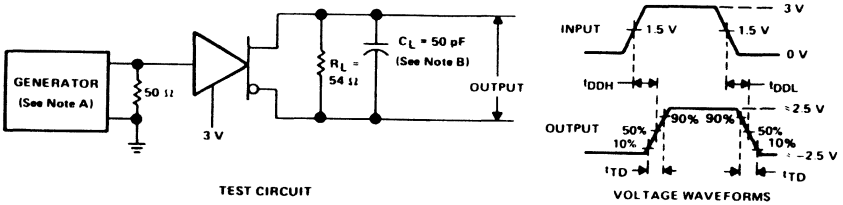


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

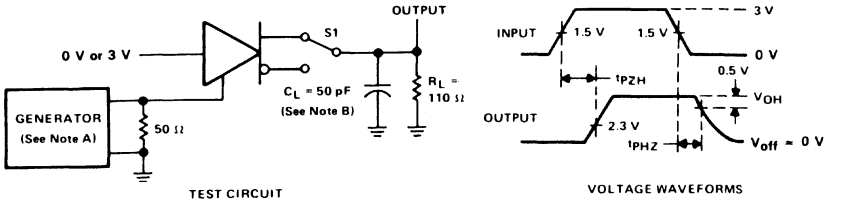


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

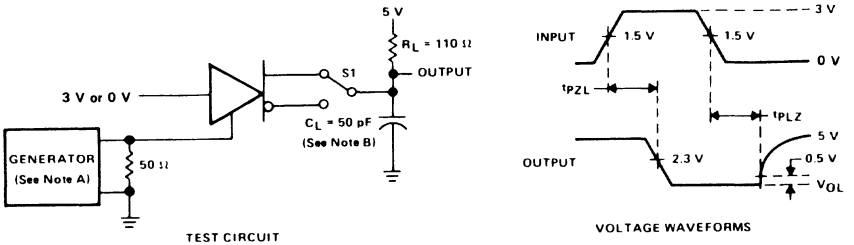


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

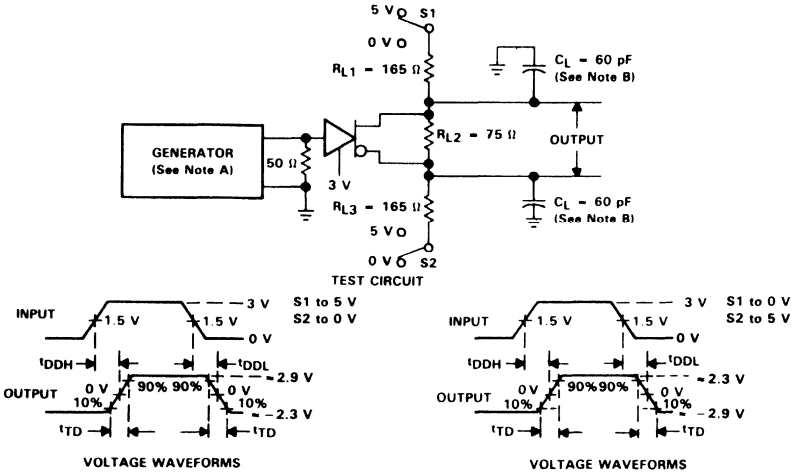
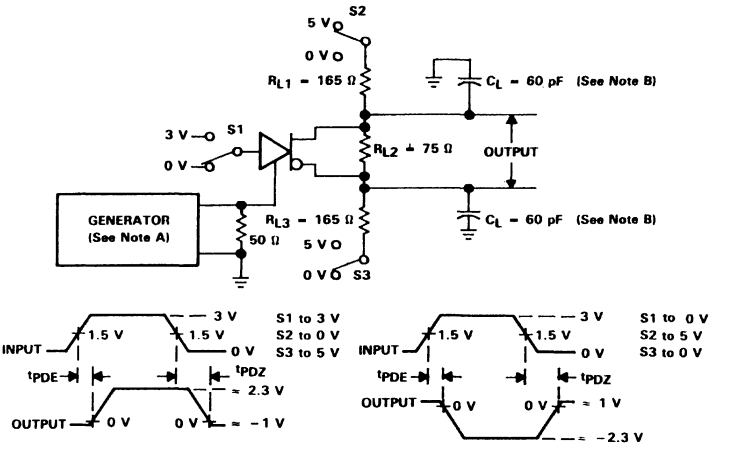


FIGURE 6. DRIVER DELAY AND TRANSITION TIMES WITH DOUBLE-DIFFERENTIAL-SCSI TERMINATION FOR THE LOAD

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 7. DRIVER DIFFERENTIAL-ENABLE AND DISABLE TIMES WITH A DOUBLE-SCSI TERMINATION

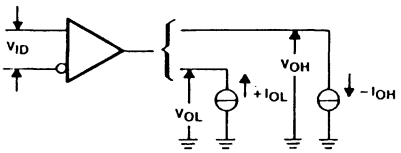


FIGURE 8. RECEIVER V_{OH} AND V_{OL}

PARAMETER MEASUREMENT INFORMATION

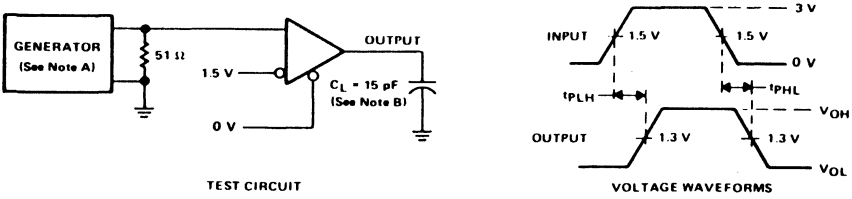


FIGURE 9. RECEIVER PROPAGATION DELAY TIMES

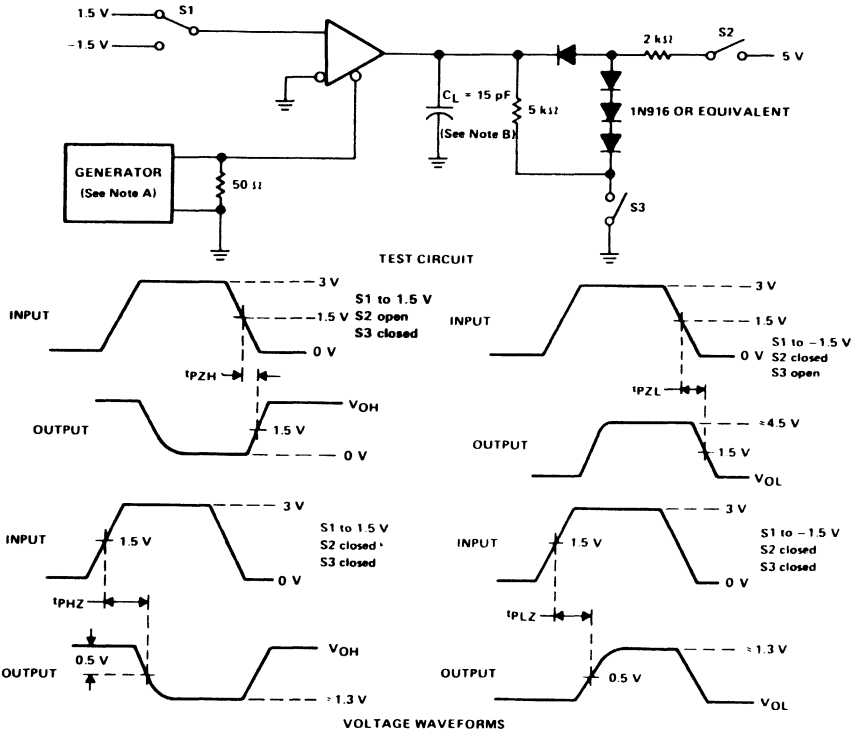


FIGURE 10. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

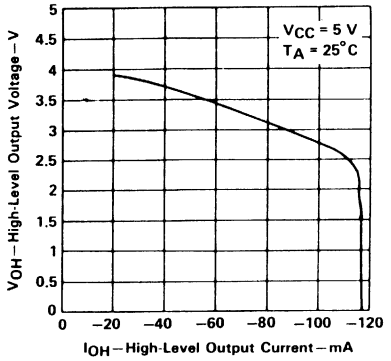


FIGURE 11

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

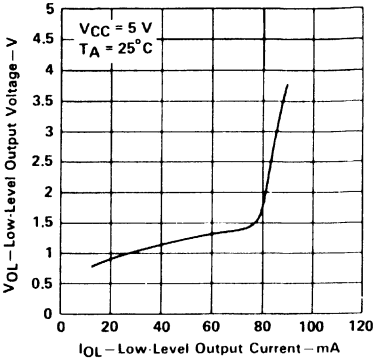


FIGURE 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

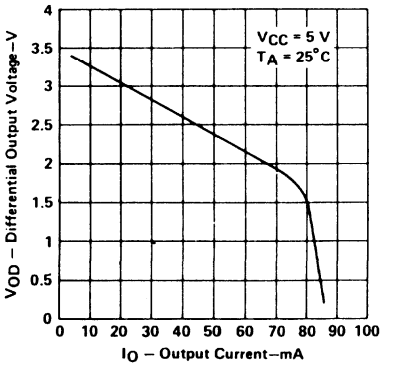


FIGURE 13

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

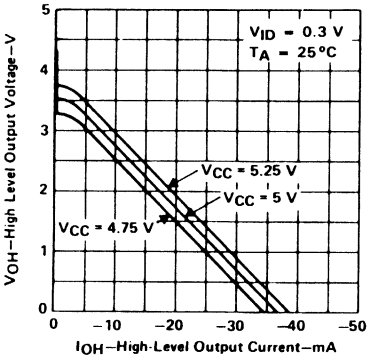


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

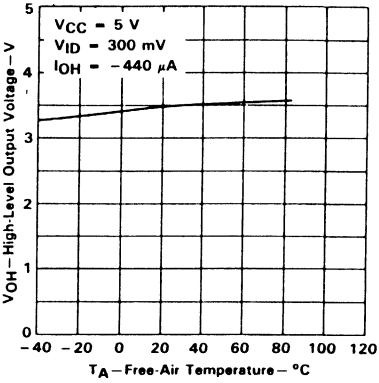


FIGURE 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

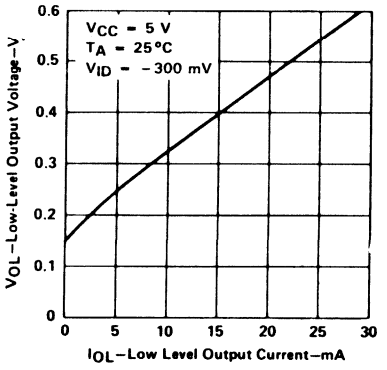


FIGURE 16

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

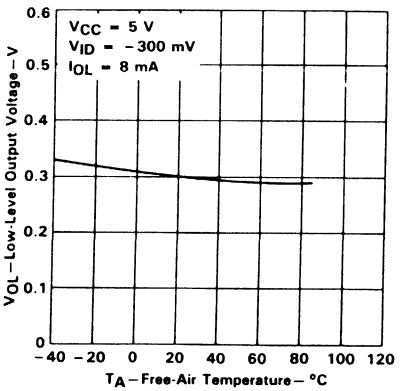


FIGURE 17

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

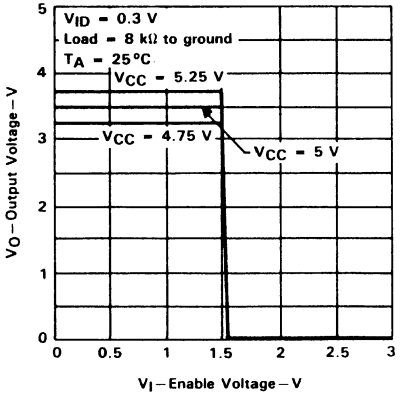


FIGURE 18

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

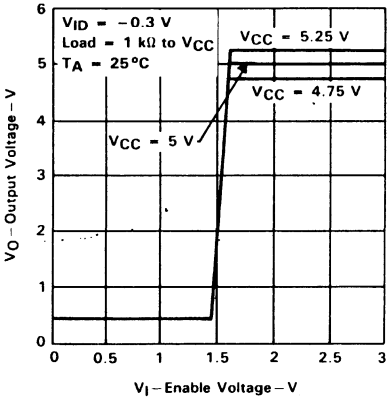


FIGURE 19

TEXAS INSTRUMENTS

APPLICATION INFORMATION

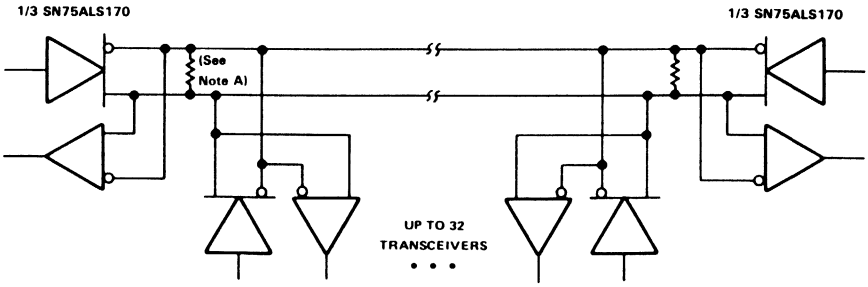


FIGURE 20. TYPICAL APPLICATION CIRCUIT

NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

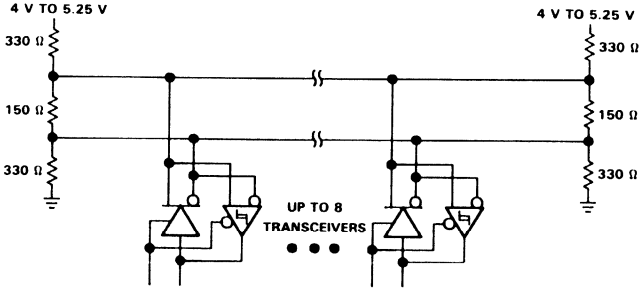


FIGURE 21. TYPICAL DIFFERENTIAL SCSI APPLICATION CIRCUIT

APPLICATION INFORMATION

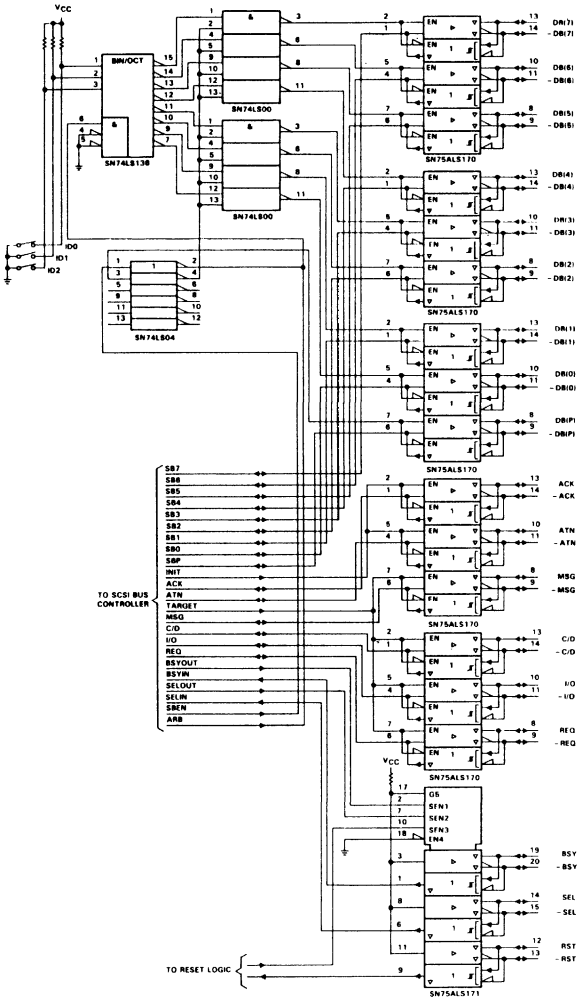
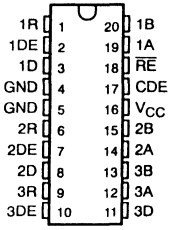


FIGURE 22. TYPICAL DIFFERENTIAL SCSI BUS INTERFACE IMPLEMENTATION

- Three Bidirectional Transceivers
- Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation In Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments
- Features Independent Driver Enables and Combined Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltages Ranges
- Driver Output Capacity . . . ± 60mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Low Supply Current Requirements
  90 mA Max

DW OR J PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLE		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

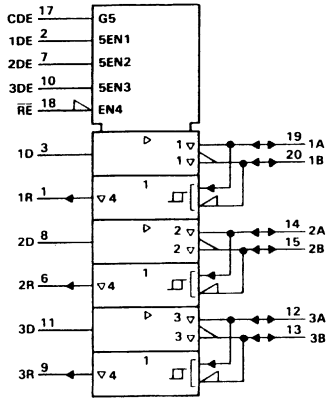
description

The SN75ALS171 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

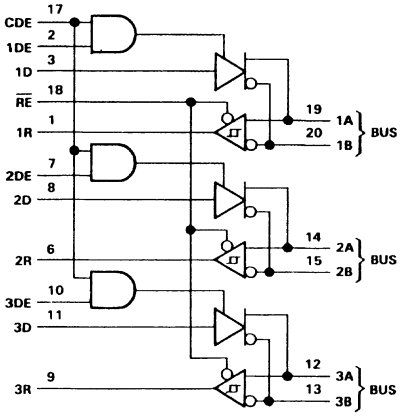
The SN75ALS171 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS171 is characterized for operation from 0°C to 70°C.

logic symbol†

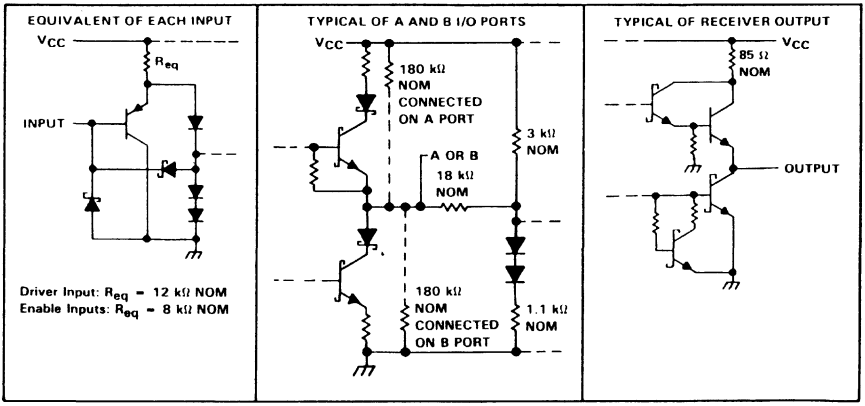


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... – 10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		– 7		12	V
High-level input voltage, V_{IH}	D, CDE, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, CDE, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			– 60	mA
	Receiver			– 400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, TA		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	$1/2\,V_{OD1}$			V
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled,	V_O = 12 V			1	mA
		See Note 3	V_O = −7 V			−0.8	
I_{IH}	High-level enable-input current	D and DE	V_{IH} = 2.7 V			20	µA
		CDE				60	
I_{IL}	Low-level enable-input current	D and DE	V_{IL} = 0.4 V			−100	
		CDE				−900	
I_{OS}	Short-circuit output current¶	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short-circuit current should not exceed one second.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)	R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	6	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6		1	6	
t_{TD}	Differential-output transition time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		30	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4	3	8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5	3	8	13	ns
t_{PDE}	Differential-output enable time	R_{L1} = R_{L3} = 165 Ω,	R_{L2} = 75 Ω,	8	30	45	ns
t_{PDZ}	Differential-output disable time	C_L = 60 pF,	See Figure 7	5	10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert V_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert V_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - V_{os} \rvert$	$\lvert V_{os} - V_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 8	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 8	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				60	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−300	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 9	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

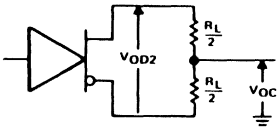


FIGURE 1. DRIVER V_{OD} AND V_{OC}

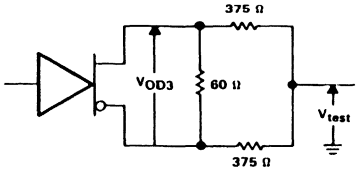


FIGURE 2. DRIVER V_{OD3}

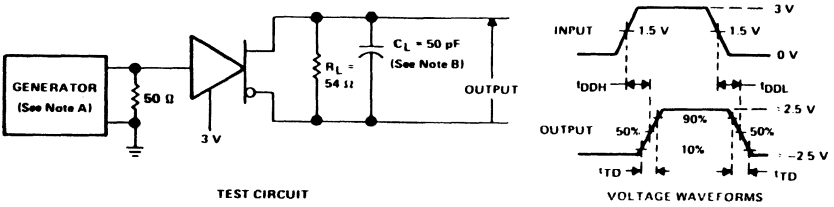


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

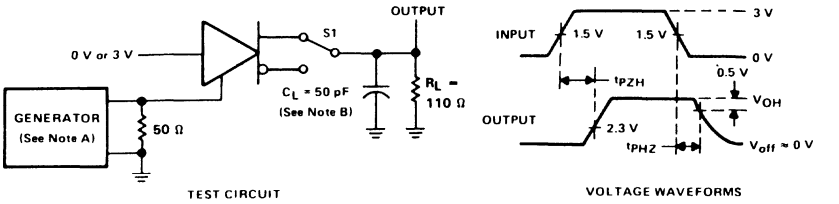


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

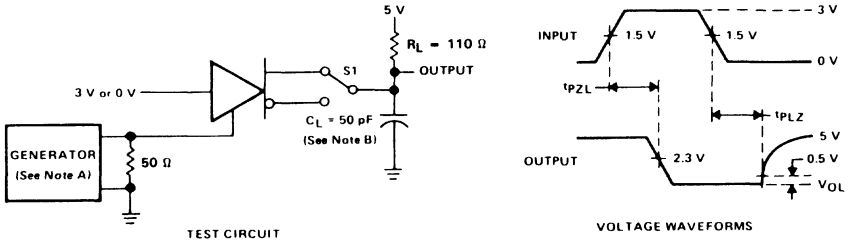


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

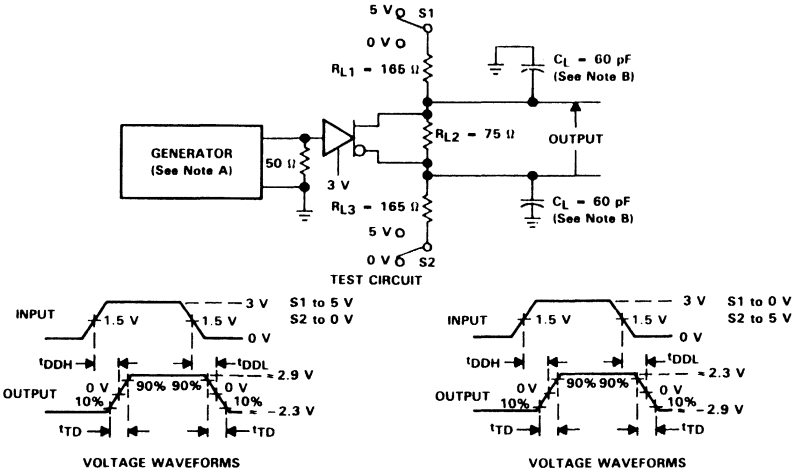


FIGURE 6. DRIVER DELAY AND TRANSITION TIMES WITH DOUBLE-DIFFERENTIAL-SCSI TERMINATION FOR THE LOAD

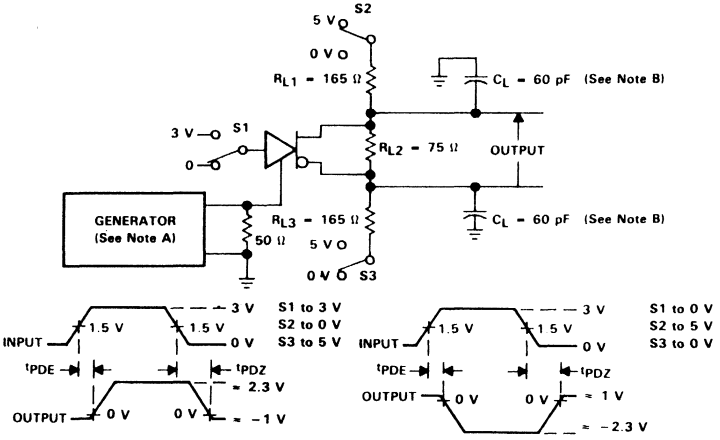


FIGURE 7. DRIVER DIFFERENTIAL-ENABLE AND DISABLE TIMES WITH A DOUBLE-SCSI TERMINATION

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

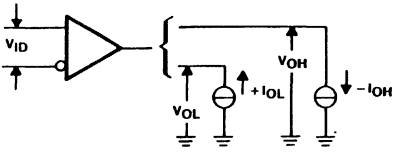


FIGURE 8. RECEIVER V_{OH} AND V_{OL}

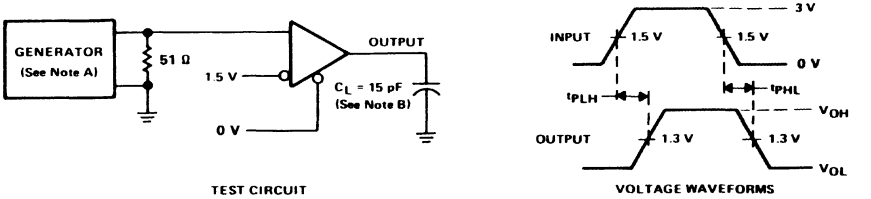


FIGURE 9. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

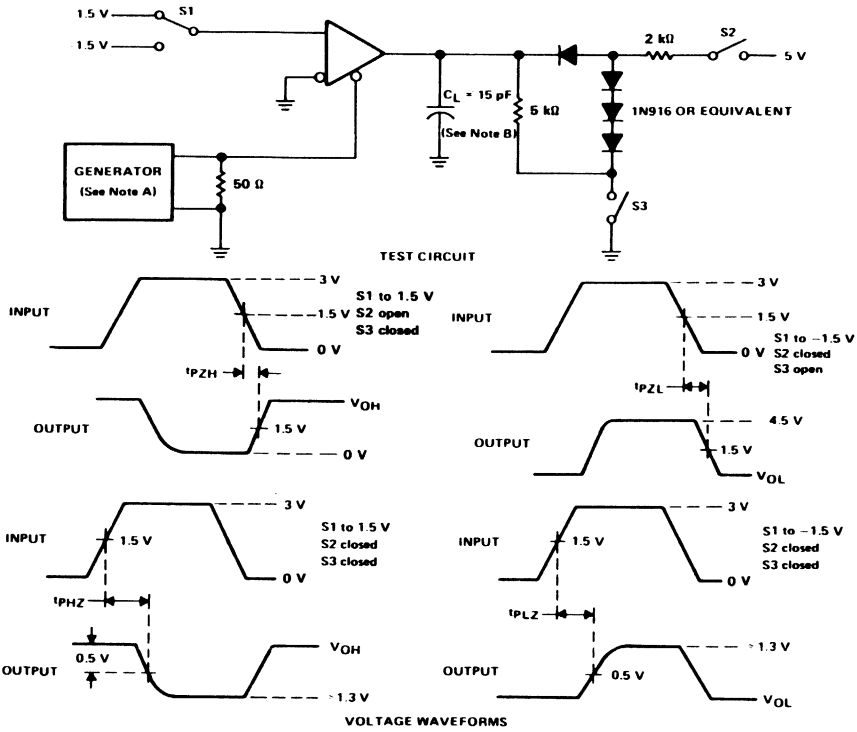


FIGURE 10. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

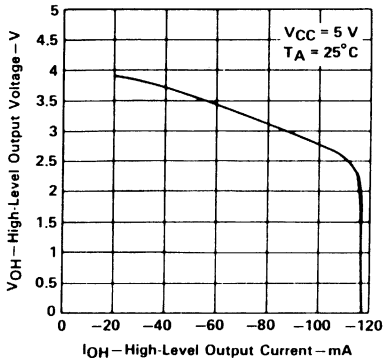


FIGURE 11

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

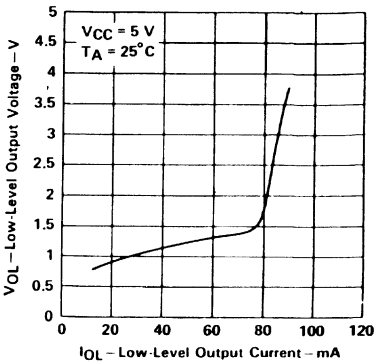


FIGURE 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

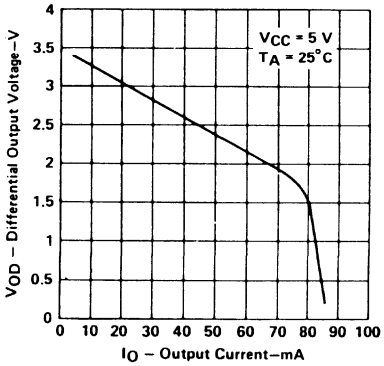


FIGURE 13

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

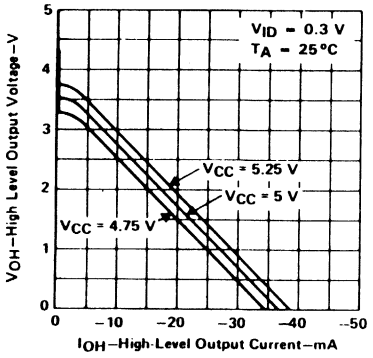


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

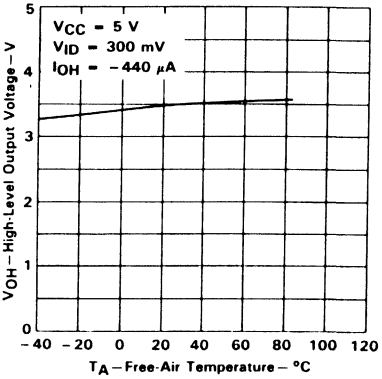


FIGURE 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

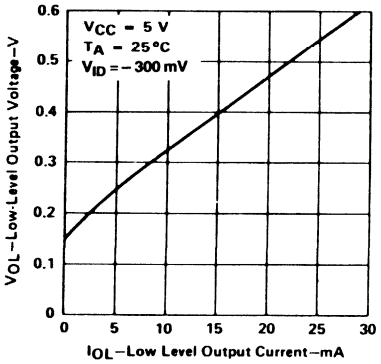


FIGURE 16

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

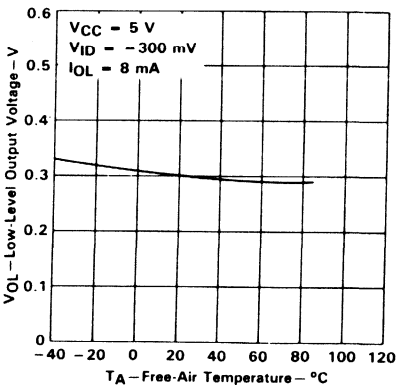


FIGURE 17

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

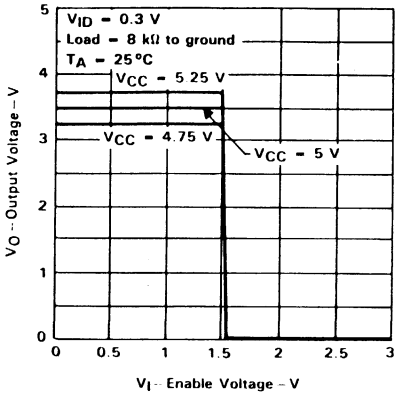


FIGURE 18

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

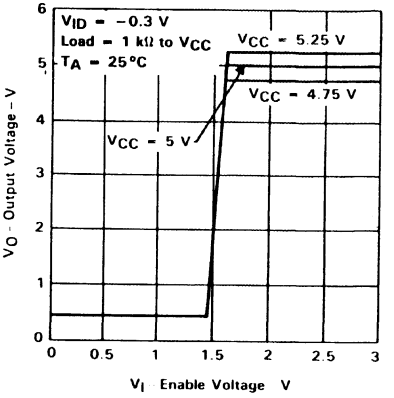
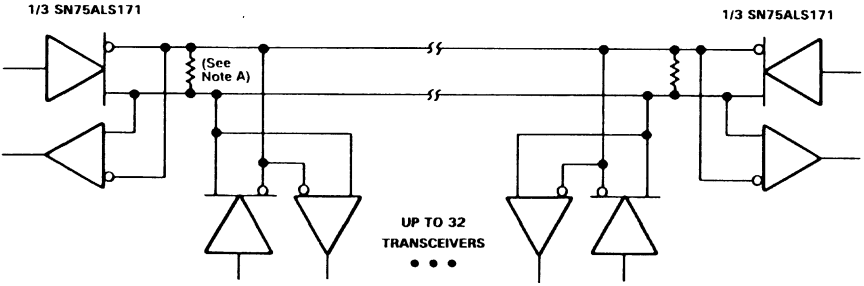


FIGURE 19

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 20. TYPICAL APPLICATION CIRCUIT

APPLICATION INFORMATION

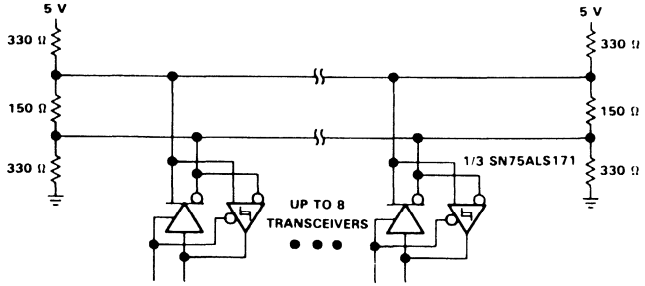


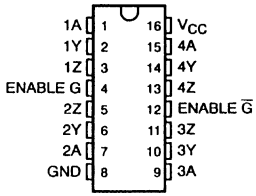
FIGURE 21. TYPICAL DIFFERENTIAL SCSI APPLICATION CIRCUIT

SN65ALS172, SN75ALS172
QUADRUPLE DIFFERENTIAL LINE DRIVERS

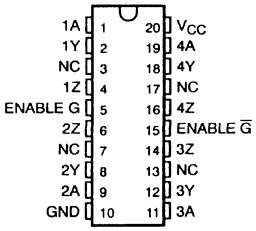
JULY 1991

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 20-MBaud Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 60 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Functionally Interchangeable with SN75172**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC–No internal connection

description

The SN65ALS172 and SN75ALS172 are quadruple line drivers with 3-state differential outputs. They are designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. These devices are optimized for balanced multipoint bus transmission at rates of up to 20 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making them suitable for party-line applications in noisy environments.

The SN65ALS172 and SN75ALS172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

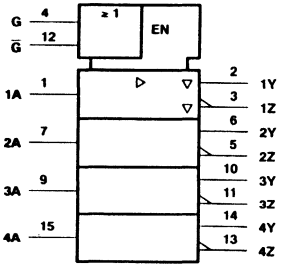
The SN65ALS172 is characterized for operation from −40°C to 85°C and the SN75ALS172 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

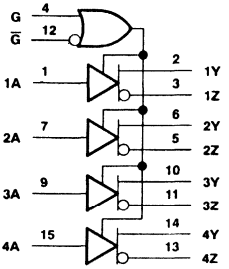
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

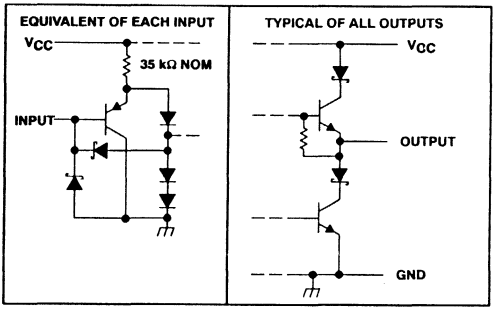


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −9 V to 14 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65ALS172 ..... −40°C to 85°C
SN75ALS172 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				+12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A	SN65ALS172	−40		85	°C
	SN75ALS172	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See Figure 1	$1/2V_{OD1}$			V
		R_L = 54 Ω		2			
				1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage§					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−100	μA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	C_L = 50 pF,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	C_L = 50 pF,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	C_L = 50 pF,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	C_L = 50 pF,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	C_L = 50 pF,	See Figure 4	10	30	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

PARAMETER MEASUREMENT INFORMATION

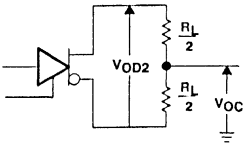
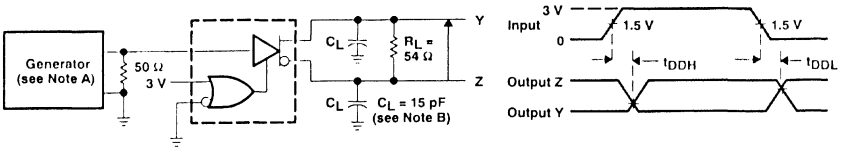


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 2. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

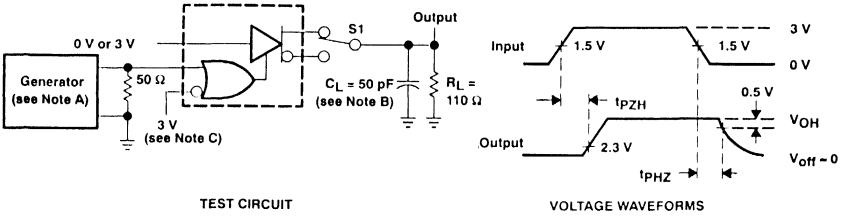


Figure 3. t_{PZH} and t_{PHZ}

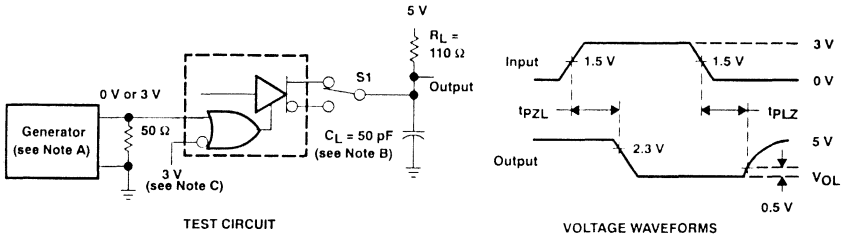


Figure 4. t_{PZL} and t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

SN75ALS173
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SEPTEMBER 1991

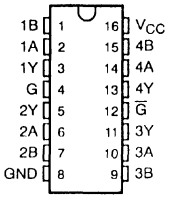
- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Log Bus Lines in Noisy Environments**
- **3-State outputs**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Supply Current Requirement 27 mA Max**

description

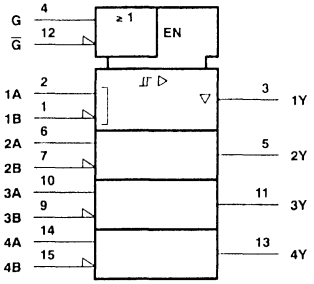
The SN75ALS173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. The four receivers have an ORed pair of enables in common. Either G being high or G being low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

The SN75ALS173 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

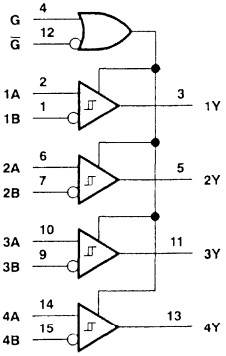


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

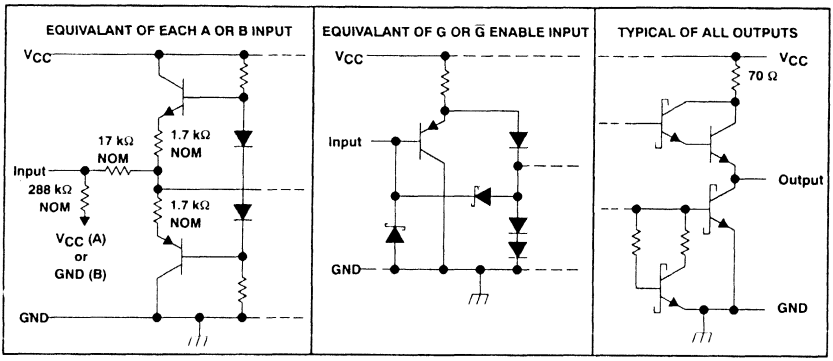


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} <$ 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs ..... ±14 V
Differential input voltage (see Note 2) ..... ±14 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level enable-input voltage, V_{IH}	2			V
Low-level enable-input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage						0.2	mV
V_{T-}	Negative-going threshold voltage				−0.2‡			mV
V_{hys}	Hysteresis§					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 1			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	See Note 4			−15		−85	mA
I_{CC}	Supply current (total package)	No load, outputs enabled				16	24	mA
		No load, outputs disabled				18	27	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,		9	18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 2	9	18	27	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 4	6	13	21	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See Figure 4	8	15	25	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

NOTES: 3. Refer to EIA Standards RS-485 for exact conditions.

4. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

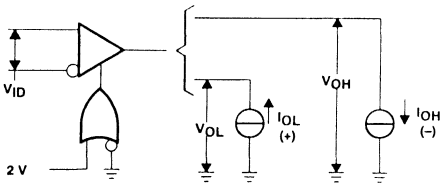


Figure 1. V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

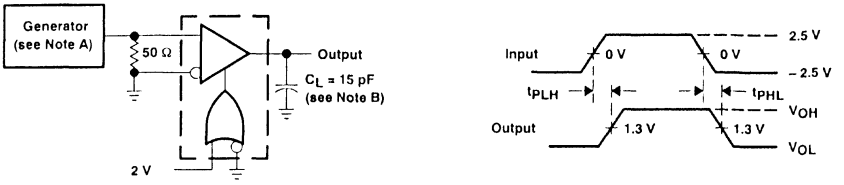


Figure 2. t_{PLH}, t_{PHL}

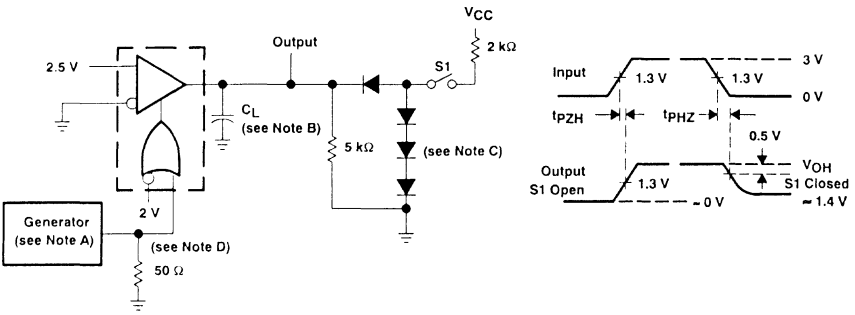


Figure 3. t_{PHZ}, t_{PZH}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

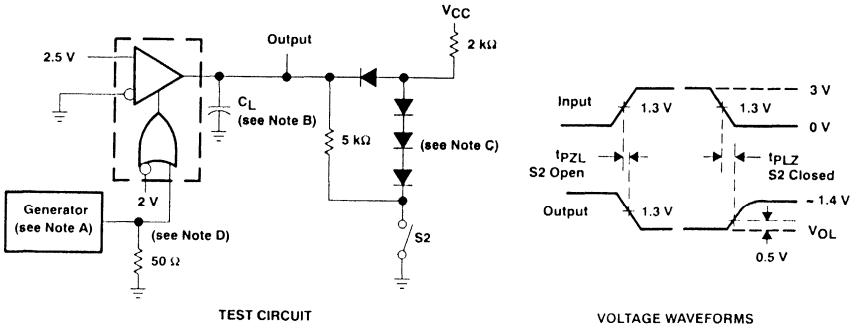


Figure 4. t_{PZL}, t_{PLZ}

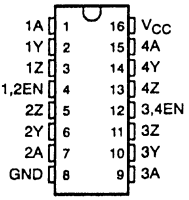
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

SN65ALS174, SN75ALS174
QUADRUPLE DIFFERENTIAL LINE DRIVERS

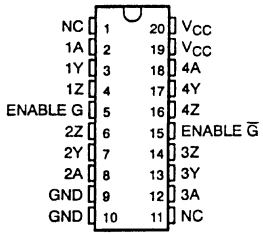
JULY 1991

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 20-MBaud Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 60 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Functionally Interchangeable with SN75174**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC–No internal connection

description

The SN65ALS174 and SN75ALS174 are quadruple line drivers with 3-state differential outputs. They are designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. These devices are optimized for balanced multipoint bus transmission at rates of up to 20 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making them suitable for party-line applications in noisy environments.

FUNCTION TABLE OF EACH DRIVER

INPUT A	ENABLES	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

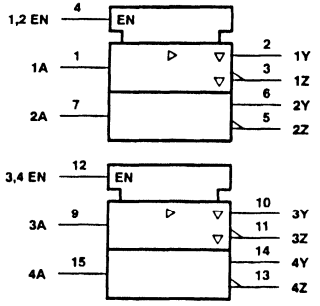
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

The SN65ALS174 and SN75ALS174 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN65ALS174 is characterized for operation from −40°C to 85°C and the SN75ALS174 is characterized for operation from 0°C to 70°C.

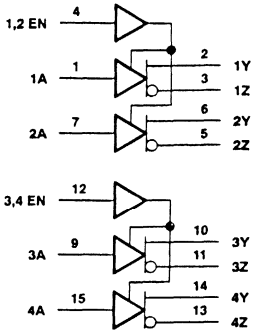
TEXAS INSTRUMENTS

logic symbol†

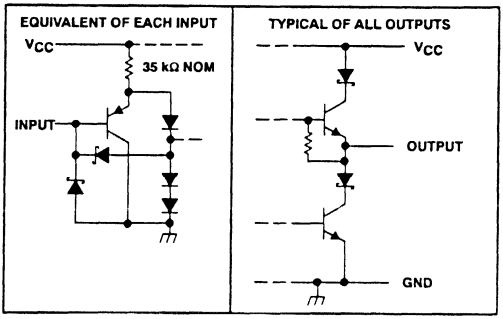


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −9 V to 14 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65ALS174 ..... −40°C to 85°C
SN75ALS174 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				+12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A	SN65ALS174	−40		85	°C
	SN75ALS174	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	$R_L = 100\ \Omega$	See Figure 1	$1/2V_{OD1}$			V
		$R_L = 54\ \Omega$		2			
				1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage§					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	μA
I_{IH}	High-level input current	$V_I = 2.7$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.5$ V				−360	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	$R_L = 54\ \Omega$,	$C_L = 50$ pF,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	$C_L = 50$ pF,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	$C_L = 50$ pF,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	$C_L = 50$ pF,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	$C_L = 50$ pF,	See Figure 4	10	30	45	ns

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

PARAMETER MEASUREMENT INFORMATION

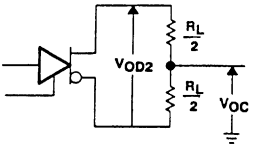
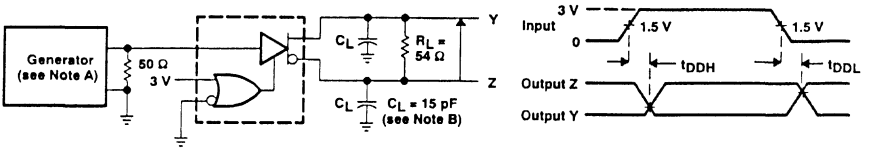


Figure 1. Differential and Common-Mode Output Voltages



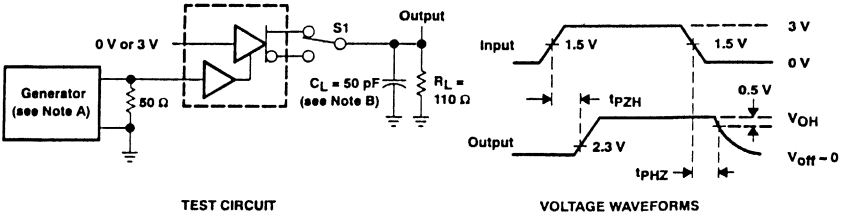
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

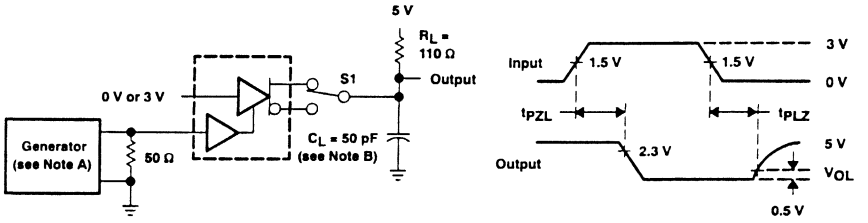
Figure 2. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. t_{PZH} and t_{PHZ}



TEST CIRCUIT VOLTAGE WAVEFORMS

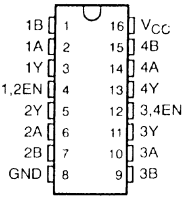
Figure 4. t_{PZL} and t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

SN75ALS175
QUAD DIFFERENTIAL LINE RECEIVERS
DECEMBER 1991

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirement 27 mA Max
- Common-Mode Input Voltage Range of −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates From Single 5-V Supply

N OR NS PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open Circuit	H	H

H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

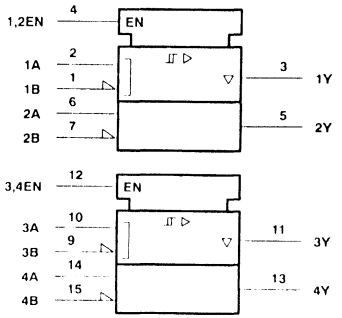
description

The SN75ALS175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Each of the two pairs of receivers has a common active-high enable. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

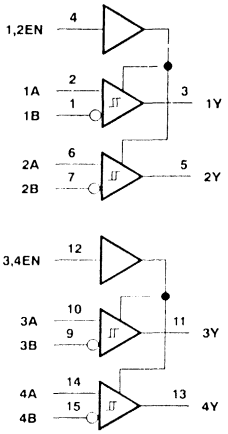
The SN75ALS175 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS

logic symbol†

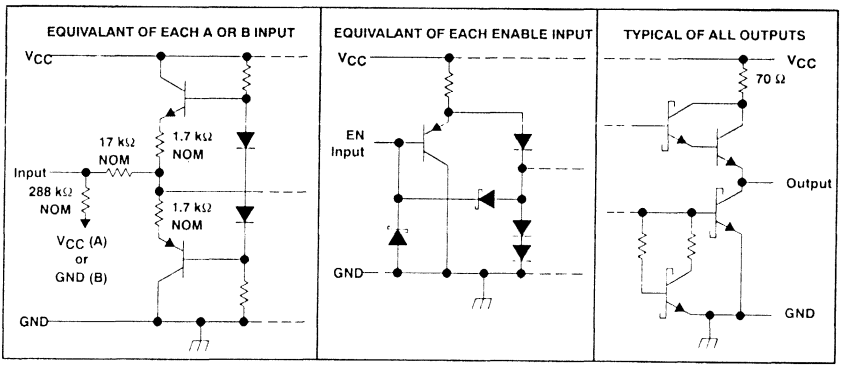


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs ..... ±14 V
Differential input voltage (see Note 2) ..... ±14 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1 150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level enable-input voltage, V_{IH}	2			V
Low-level enable-input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	µA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage						200	mV
V_{T-}	Negative-going threshold voltage				−200‡			mV
V_{hys}	Hysteresis§					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 1			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	$V_{IH(E)}$ = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	$V_{IL(E)}$ = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_O = 0,	See Note 4		−15		−85	mA
I_{CC}	Supply current (total package)	No load,	Outputs enabled			16	24	mA
		No load,	Outputs disabled			18	27	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

NOTES: 3. Refer to EIA Standards RS-485 for exact conditions.

4. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,		9	18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 2	9	18	27	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level			6	13	21	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level			8	15	25	ns

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

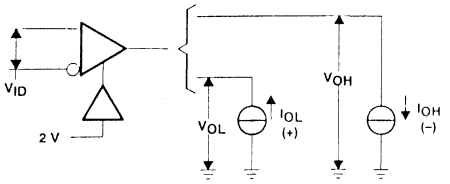


Figure 1. V_{OH}, V_{OL}

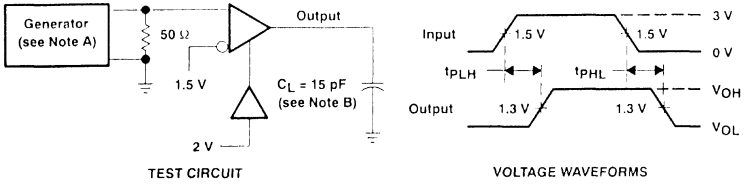


Figure 2. Propagation Delay Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, t_r = t_f = 6 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

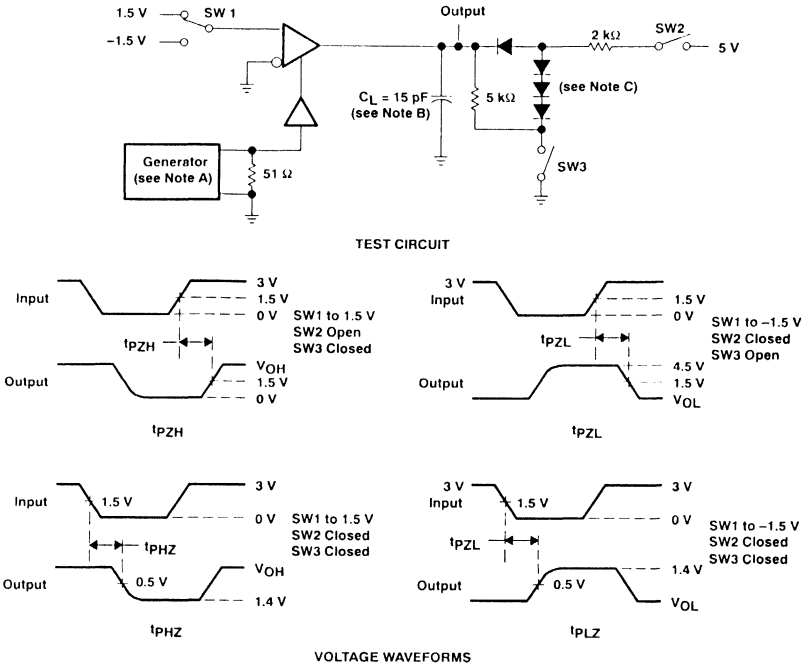


Figure 3. Enable and Disable Times

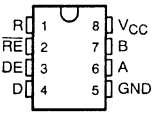
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, t_r = t_f = 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

AUGUST 1991

- Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed and Tested for Data Rates Up to 35 MBaud
- SN65ALS176 Operating Temperature −40°C to 85°C
- Three Skew Limits Available:
  - 'ALS176 . . . 10 ns
  - 'ALS176A . . . 7.5 ns
  - 'ALS176B . . . 5 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 30 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

T_A	$t_{pmax} - t_{pmin}$	PACKAGE	
	$t_{sk(LIM)}$‡	SMALL OUTLINE (D)†	PLASTIC DIP (P)
0°C to 70°C	10	SN75ALS176D	SN75ALS176P
	7.5	SN75ALS176AD	SN75ALS176AP
	5	SN75ALS176BD	SN75ALS176BP
−40°C to 85°C	10	SN65ALS176D	SN65ALS176P

† The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75ALS176DR).

‡ $t_{sk(LIM)}$ is the greater of 1) the difference between the maximum and minimum specified values of t_{PLH} (or t_{DDH}), and 2) the difference between the maximum and minimum specified values of t_{PHL} (or t_{DDL}). This is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device-to-device.

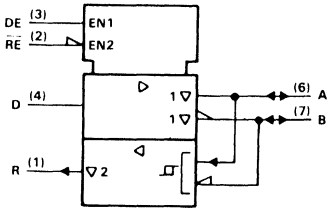
description

The SN65ALS176 and SN75ALS176 series Differential Bus Transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

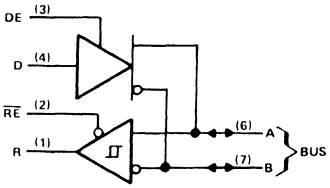
The SN65ALS176 and SN75ALS176 series combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from −40°C to 85°C and the SN75ALS176 series is characterized for operation from 0°C to 70°C.

logic symbol†

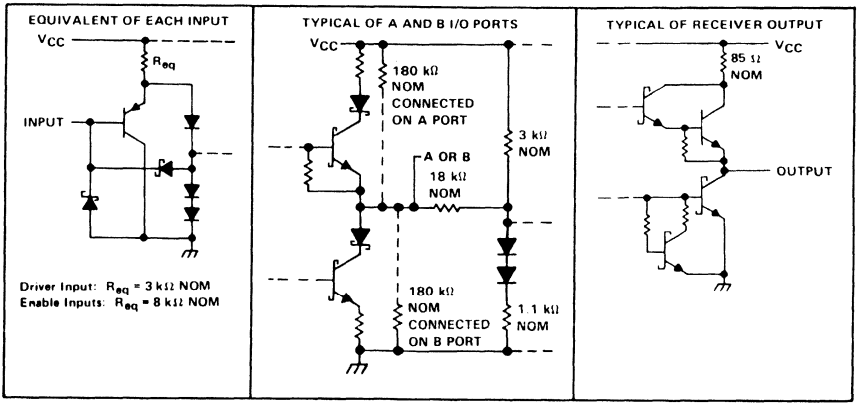


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −7 V to 12 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS176 ..... −40°C to 85°C
SN75ALS176 Series ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PARAMETER	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS176	−40		85	°C
	SN75ALS176	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	$1/2\,V_{OD1}$			
				2			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled,	$V_O = 12$ V			1	mA
		See Note 3	$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current	$V_O = -4$ V	SN65ALS176			−250	mA
		$V_O = -6$ V	SN75ALS176				
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 8$ V					
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{DD}	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3			15	ns
$t_{sk(p)}$	Pulse skew ($\|t_{DDL} - t_{DDH}\|$)			0	2	ns
t_{TD}	Differential output transition time			8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{DD}	Differential output delay time	'ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3	3	8	13	ns
		'ALS176A		4	7	11.5	
		'ALS176B		5	8	10	
$t_{sk(p)}$	Pulse skew ($\|t_{DDL} - t_{DDH}\|$)				0	2	ns
t_{TD}	Differential output transition time				8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7			25	ns
$t_{sk(p)}$	Pulse skew (| $t_{PHL} - t_{PLH}$ |)			0	2	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		11	18	ns
t_{PZL}	Output enable time to low level			11	18	ns
t_{PHZ}	Output disable time from high level				50	ns
t_{PLZ}	Output disable time from low level				30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	9	14	19	ns
		'ALS176A		10.5	14	18	
		'ALS176B		11.5	13	16.5	
$t_{sk(p)}$	Pulse skew (| $t_{PHL} - t_{PLH}$ |)				0	2	ns
t_{PZH}	Output enable time to high level		C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level				20	35	ns
t_{PHZ}	Output disable time from high level				20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

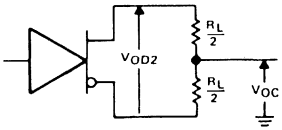


Figure 1. Driver V_{OD} and V_{OC}

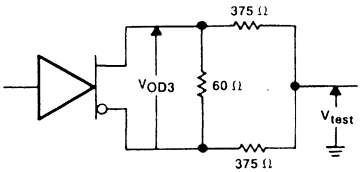
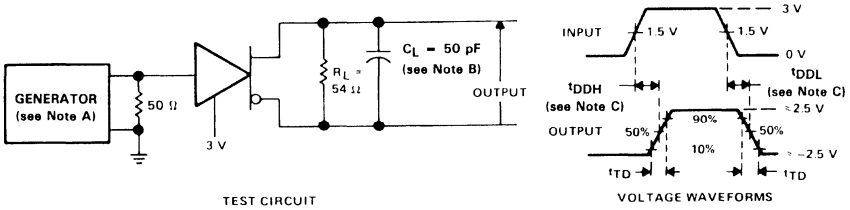


Figure 2. Driver V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. t_{DD} = t_{DDH} or t_{DDL}

Figure 3. Driver Differential-Output Delay and Transition Times

PARAMETER MEASUREMENT INFORMATION

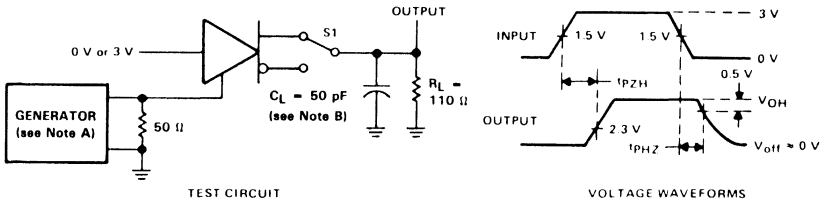


Figure 4. Driver Enable and Disable Times

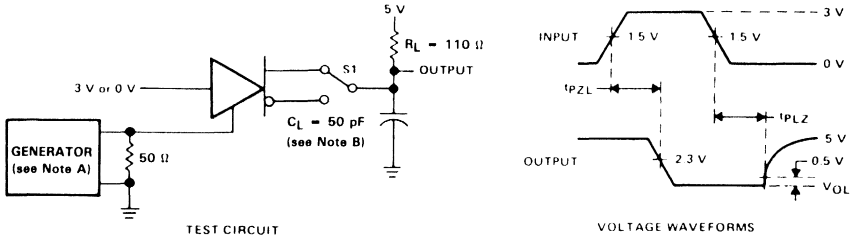


Figure 5. Driver Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

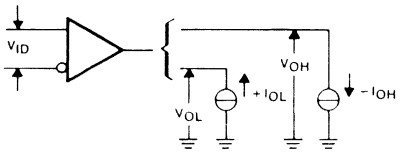


Figure 6. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

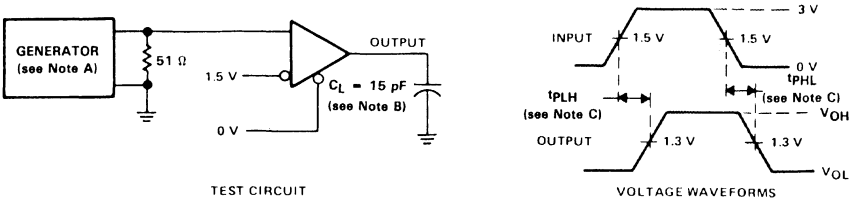


Figure 7. Receiver Propagation Delay Times

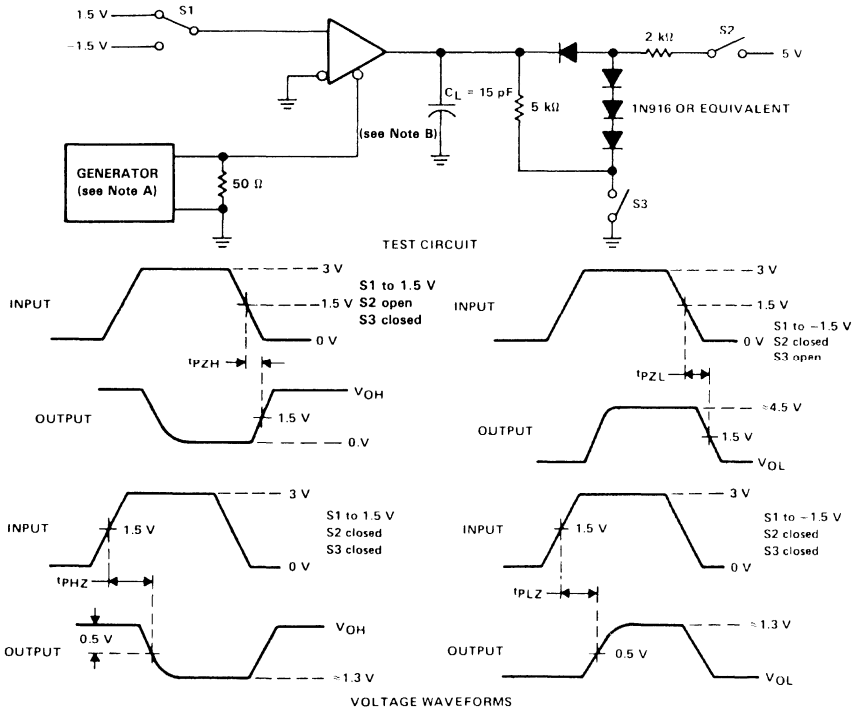


Figure 8. Receiver Output Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. $t_{pd} = t_{PLH}$ or t_{PHL}

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

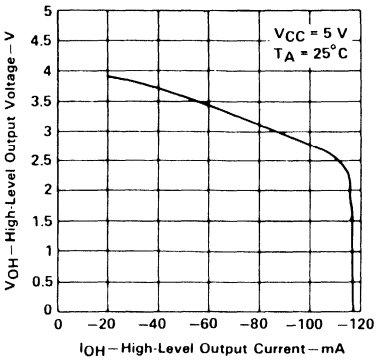


Figure 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

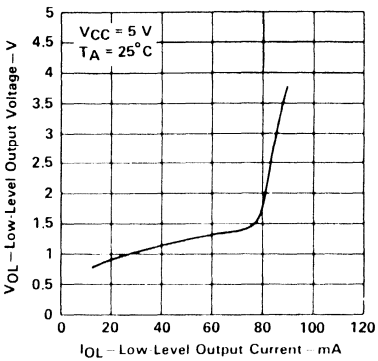


Figure 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

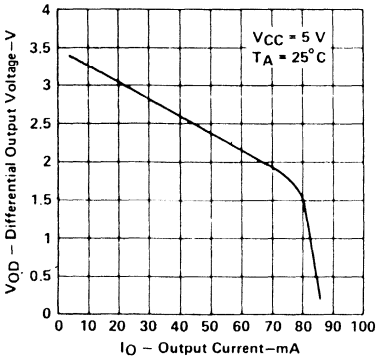


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

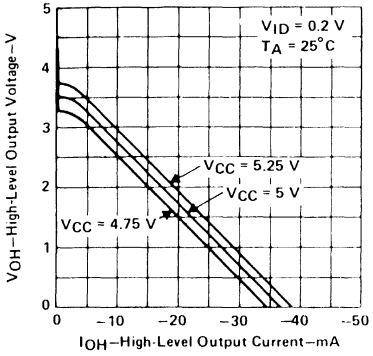


Figure 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

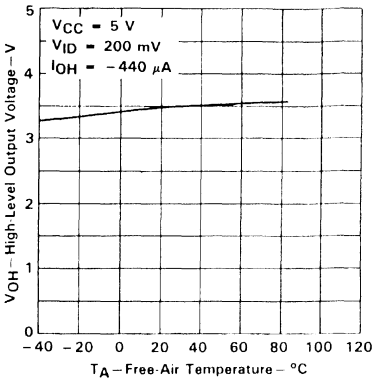


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

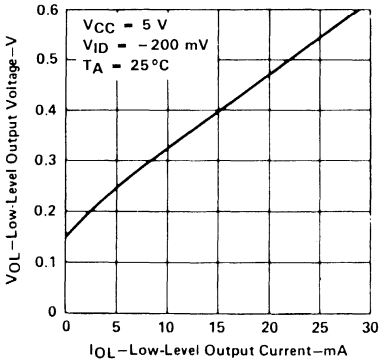


Figure 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

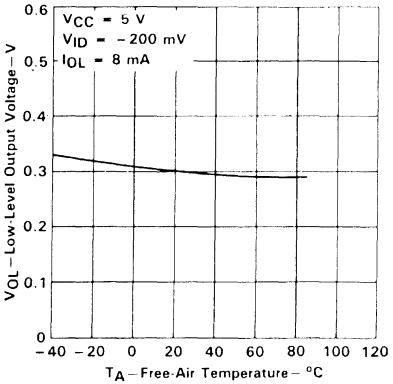


Figure 15

TYPICAL CHARACTERISTICS

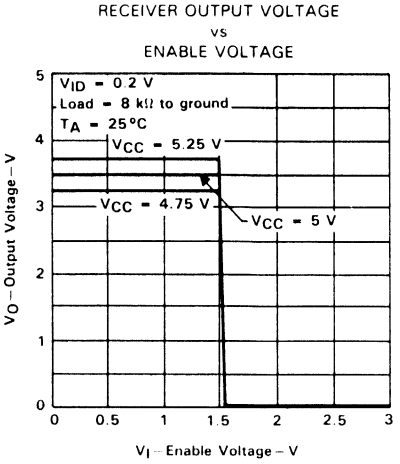


Figure 16

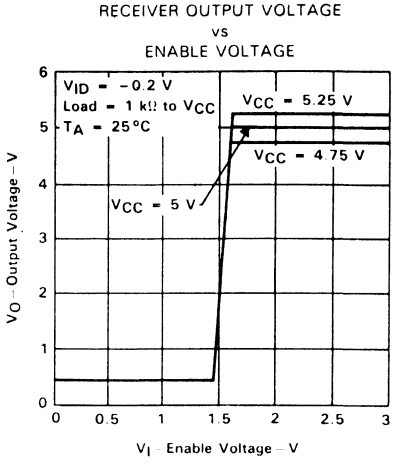


Figure 17

APPLICATION INFORMATION

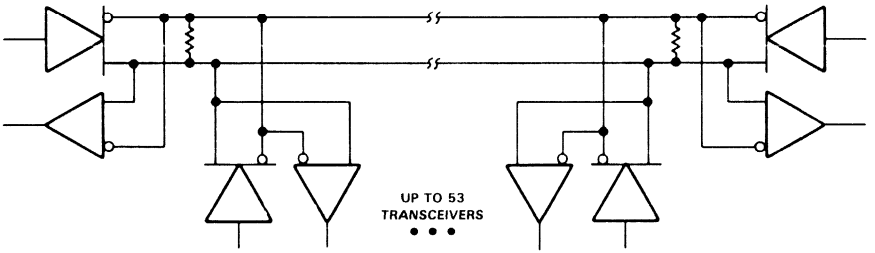


Figure 18. Typical Application Circuit

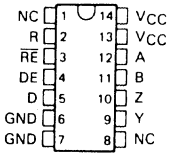
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

SN65ALS180, SN75ALS180
DIFFERENTIAL DRIVER AND RECEIVER PAIRS

DECEMBER 1989

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation In Both Serial and Parallel Applications
- Low Skew between Devices . . . 6 ns Max
- Low Supply Current Requirements 30 mA Max
- Individual Driver and Receiver I/O pins with Dual V_{CC} and Dual GND
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} <$ 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

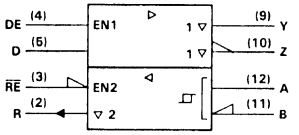
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

escription

The SN65ALS180 and SN75ALS180 Differential Driver and Receiver Pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

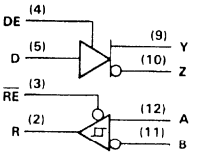
The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

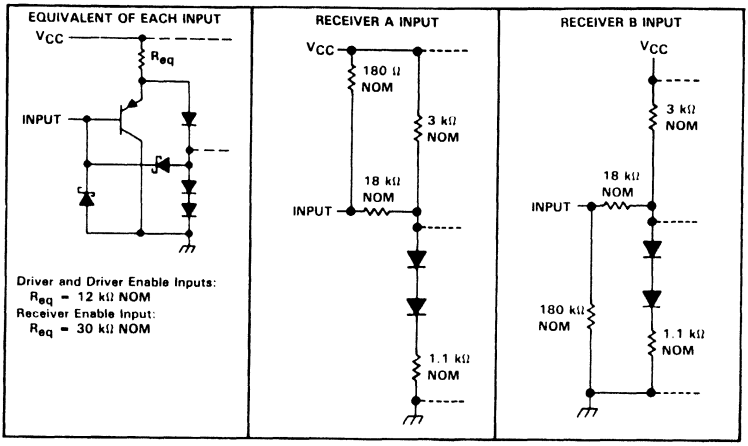


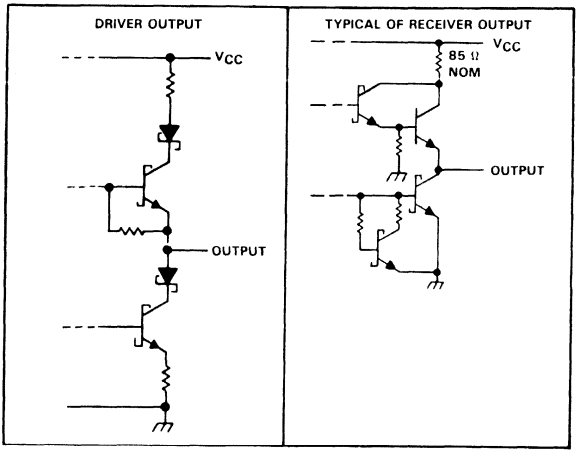
TEXAS INSTRUMENTS

minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from −40°C to 85°C and the SN75ALS180 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS180 . . . . . −40°C to 85°C
SN75ALS180 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

			MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12 −7	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$		2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$				0.8	V
Differential input voltage, V_{ID} (see Note 2)					±12	V
High-level output current, I_{OH}	Driver				−60	mA
	Receiver				−400	µA
Low-level output current, I_{OL}	Driver				60	mA
	Receiver				8	
Operating free-air temperature, T_A		SN65ALS180	−40		85	°C
		SN75ALS180	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A/Y with respect to the inverting terminal B/Z.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3 −1	V
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled,	V_O = 12 V			1	mA
		See Note 3	V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current¶	V_O = −7 V	SN75ALS180			−250	mA
		V_O = −6 V	SN65ALS180				
		V_O = 0	All			−150	
		V_O = V_{CC}	All				
		V_O = 8 V	SN65ALS180			250	
		V_O = 12 V	SN75ALS180				
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

¶ Duration of the short circuit should not exceed one second.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		3	8	13	ns
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)				1	6	ns
t_{TD}	Differential output transition time			3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		19	24	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		8	13	ns

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \bar{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \bar{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \bar{V}_{os} \rvert$	$\lvert V_{os} - \bar{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 7, C_L = 15 pF	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output		9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level			7	14	ns
t_{PHZ}	Output disable time from high level			20	35	ns
t_{PLZ}	Output disable time from low level			8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

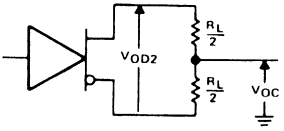


FIGURE 1. DRIVER V_{OD} AND V_{OC}

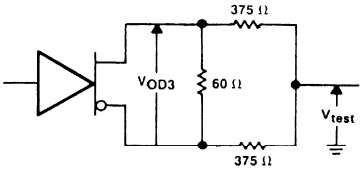


FIGURE 2. DRIVER V_{OD3}

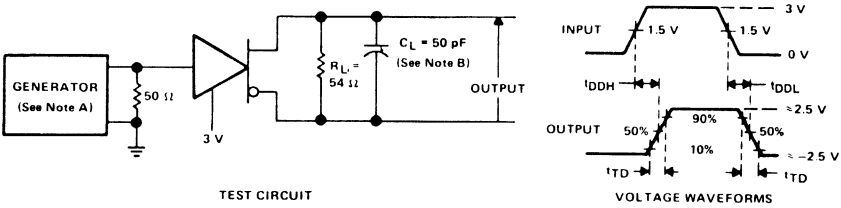


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

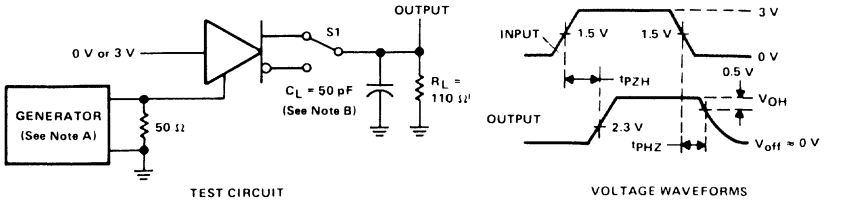


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

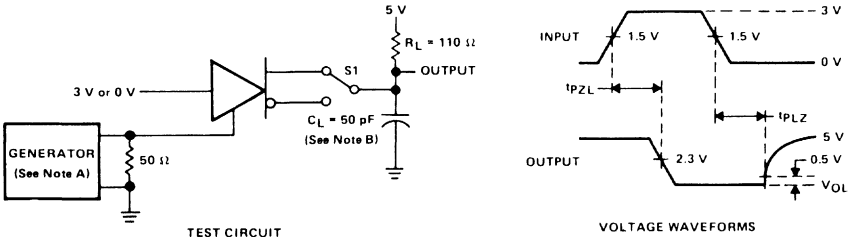


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

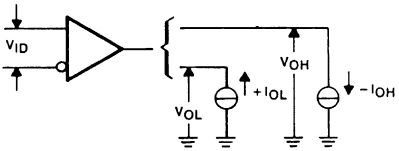


FIGURE 6. RECEIVER V_{OH} AND V_{OL}

PARAMETER MEASUREMENT INFORMATION

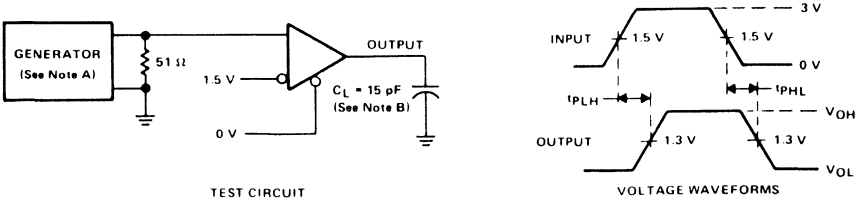


FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

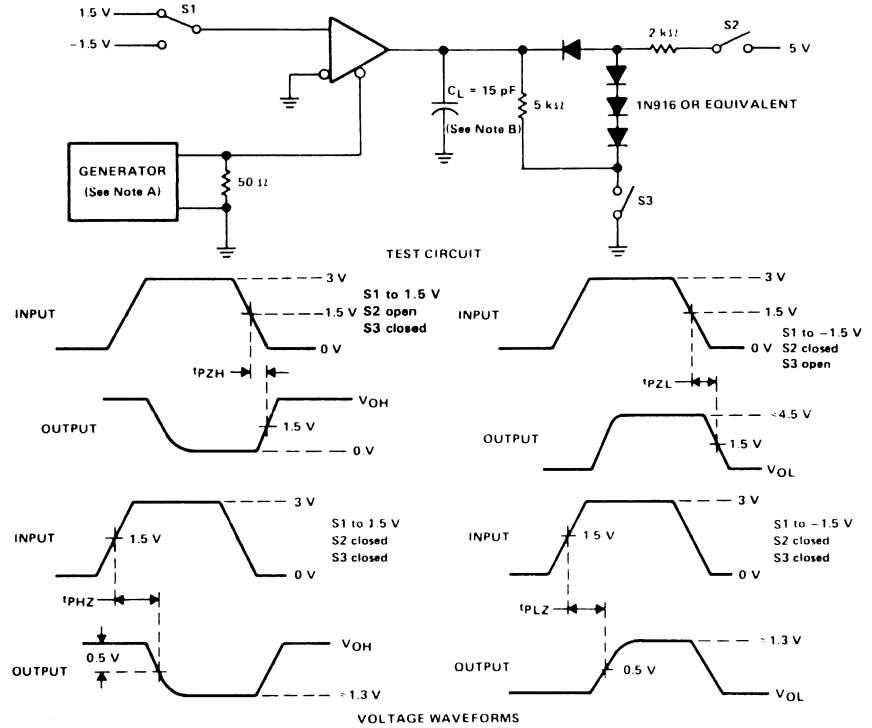


FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 5 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

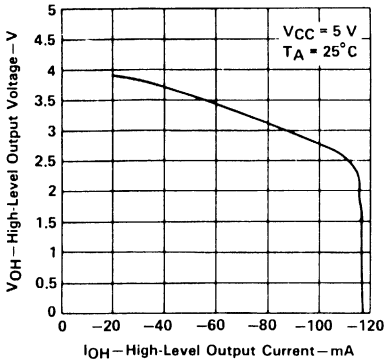


FIGURE 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

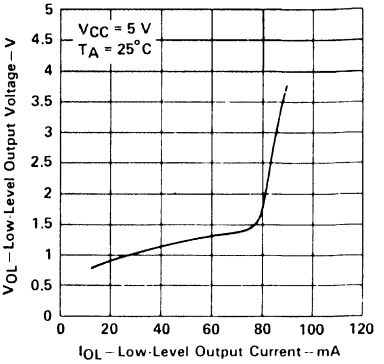


FIGURE 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

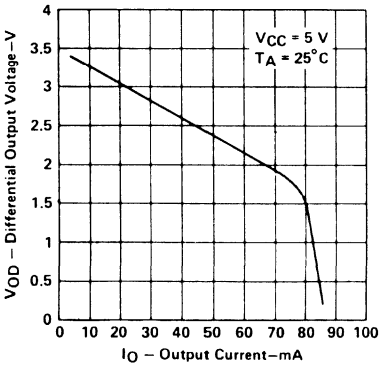


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

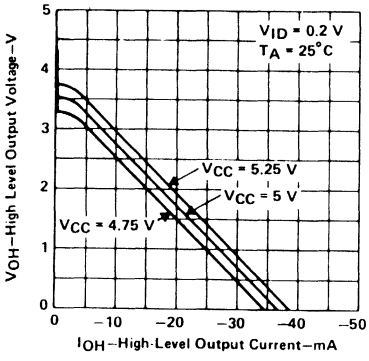


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

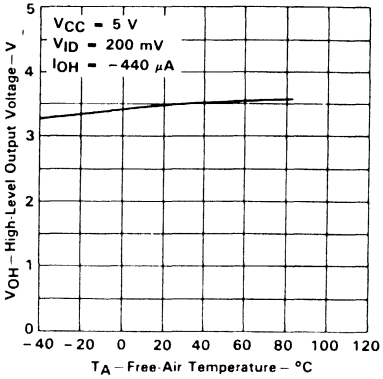


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

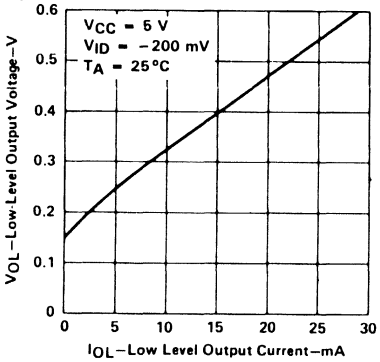


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

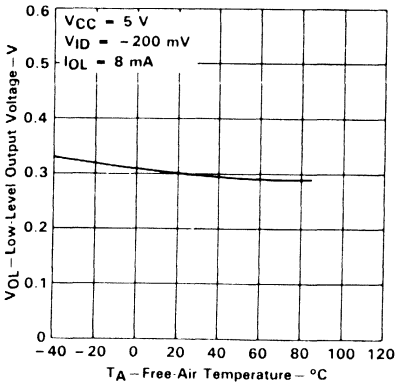


FIGURE 15

SN75ALS191
DUAL DIFFERENTIAL LINE DRIVER

AUGUST 1989

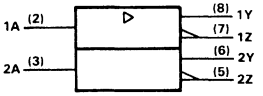
- **Meets EIA Standard RS-422-A**
- **High Speed, Low-Power ALS Design**
- **TTL-and CMOS-Input Compatibility**
- **Single 5-V Supply Operation**
- **Output Short-Circuit Protection**
- **Improved Replacement for the UA9638**

description

The SN75ALS191 is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-volt power supply and is supplied in 8-pin packages.

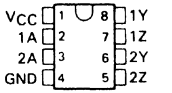
The SN75ALS191 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

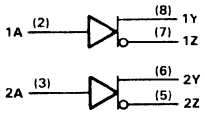
D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

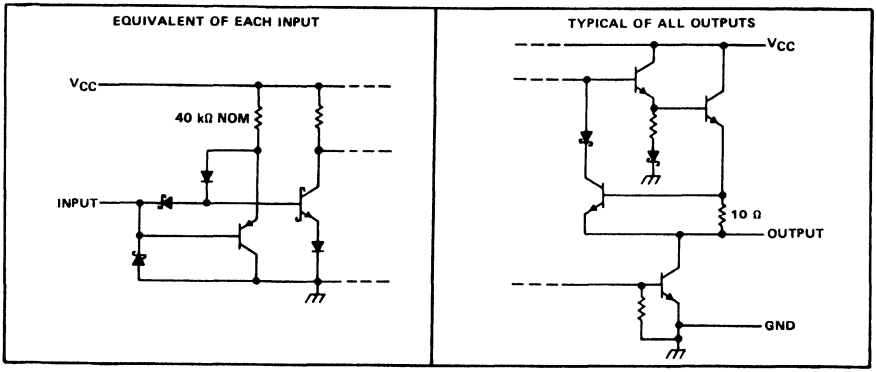
INPUT	OUTPUTS	
A	Y	Z
H	H	L
L	L	H

logic diagram (positive logic)



TEXAS INSTRUMENTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.3		V
			I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 1		2			V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of‡ differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of‡ common-mode output voltage					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0		−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, No load,	All inputs at 0 V		32	40	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		TEST CONDITION	MIN	TYP#	MAX	UNIT
t_{DD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		3.5	7	ns
t_{TD}	Differential-output transition time			3.5	7	ns
	Skew			1.5	4	ns

Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

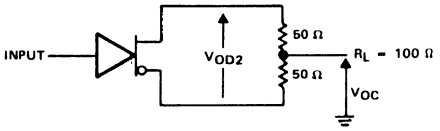
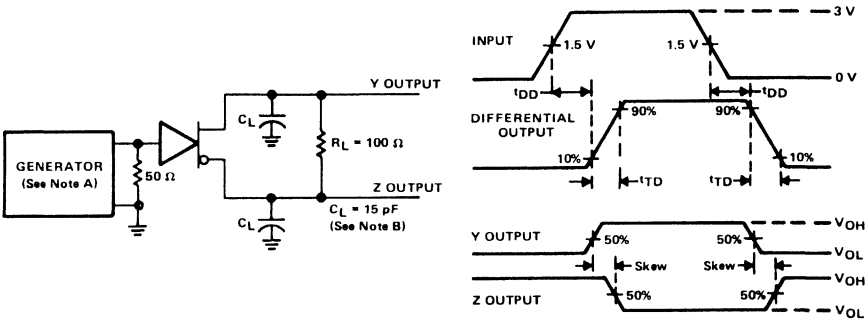


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

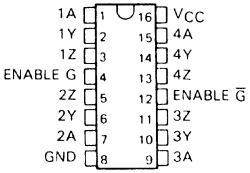
FIGURE 2. SWITCHING TIMES

SN55ALS192, SN75ALS192
QUADRUPLE DIFFERENTIAL LINE DRIVERS

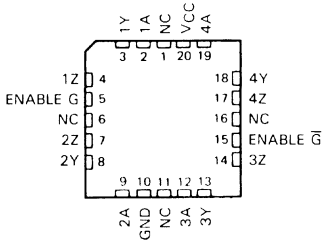
JUNE 1986

- **Meets EIA Standard RS-422-A**
- **High-Speed, Low-Power ALS Design**
- **3-State TTL Compatible**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Complementary Output Enable Inputs**
- **Improved Replacement for the AM26LS31**

SN55ALS192 . . . J PACKAGE
SN75ALS192 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55ASL192 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple complementary-output line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

High-impedance inputs maintain input currents low, less than 1 μA for a high level and less than 100 μA for a low level. Complementary control inputs, G and $\overline{G}$, allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver. The SN55ALS192 is also capable of data rates in excess of 20 megabits per second and designed to operate with the SN55ALS193; however, it may be limited to a lower bit rate based on the temperature. Reference should be made to the Dissipation Rating Table and Figure 15.

The SN55ALS192 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75ALS192 is characterized for operation from 0°C to 70°C.

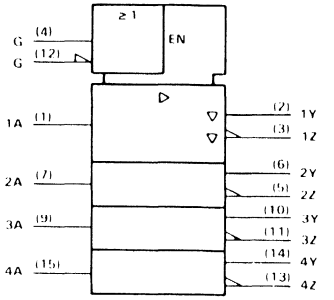
FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

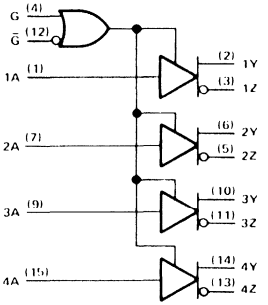
H = high level, L = low level,
Z = high impedance (off),
X = irrelevant

TEXAS INSTRUMENTS

logic symbol†

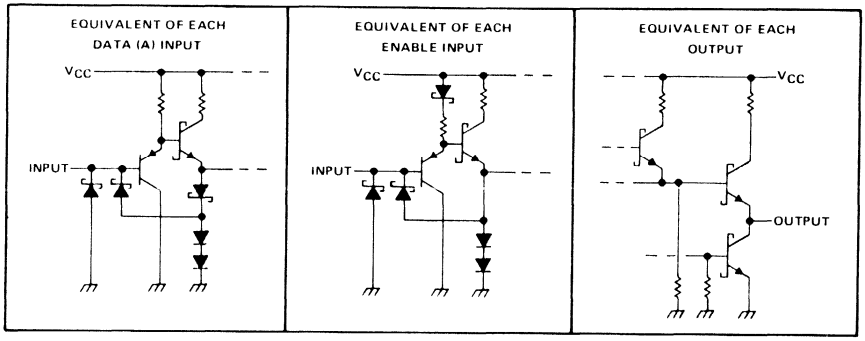


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55ALS192	SN75ALS192	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I		7	7	V
Output off-state voltage		6	6	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	D package		950	mW
	FK package	1375		
	J package	1375	1025	
	N package		1150	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Rating Table. In the J package, SN55ALS192 chips are either alloy or silver glass mounted and SN75ALS192 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	
FK or J (SN55ALS912)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS192)	1025 mW	8.2 mW/°C	656 mW	
N	1150 mW	9.2 mW/°C	736 mW	

recommended operating conditions

	SN55ALS192			SN75ALS192			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−20			−20	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55ALS192			SN75ALS192			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High level output voltage	V_{CC} = MIN, I_{OH} = −20 mA		2.4			2.5			V
V_{OL}	Low level output voltage	V_{CC} = MIN, I_{OL} = 20 mA				0.5			0.5	V
V_O	Output voltage	V_{CC} = MAX, I_O = 0		0		6	0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MIN, I_O = 0		1.5		6	1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			½ V_{OD1}			V
				2			2			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 100 Ω, See Figure 1				±0.2			±0.2	V
V_{OC}	Common mode output voltage¶					±3			±3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common mode output voltage§					±0.2			±0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100			100	μA
			V_O = −0.25 V			100			100	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX	V_O = 0.5 V			−20			−20	μA
			V_O = 2.5 V			20			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low level input current	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−30		−150	−30		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX, All outputs disabled			26	45		26	45	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS 422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, S1 and S2 open		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	ns
	Output-to-output skew			3	6	ns
t_{PZH}	Output enable time to high level	R_L = 75 Ω		11	15	ns
t_{PZL}	Output enable time to low level	R_L = 180 Ω		16	20	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, S1 and S2 closed		8	15	ns
t_{PLZ}	Output disable time from low level			18	20	ns

PARAMETER MEASUREMENT INFORMATION

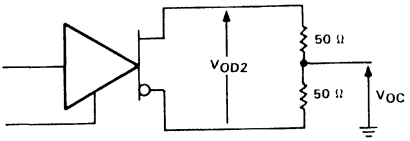
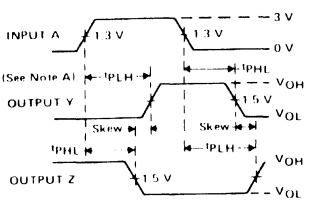
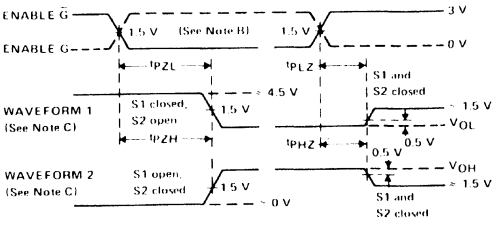


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

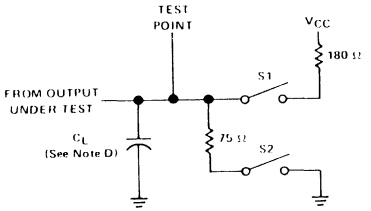


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.

FIGURE 2. SWITCHING TIMES

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

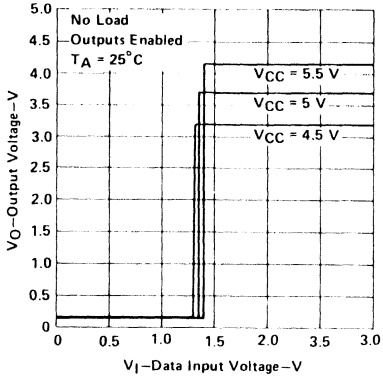


FIGURE 3

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

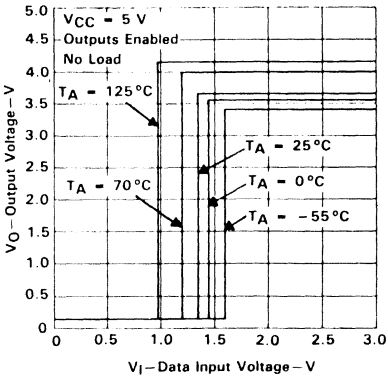


FIGURE 4

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

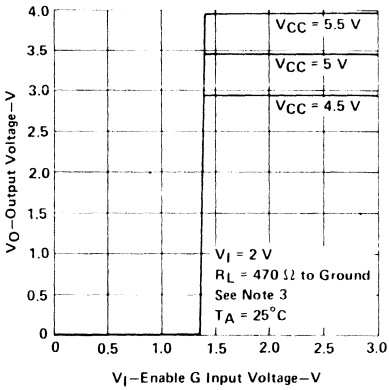


FIGURE 5

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

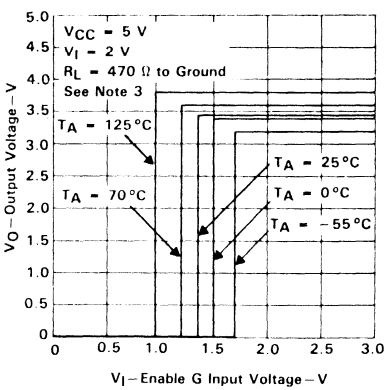


FIGURE 6

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

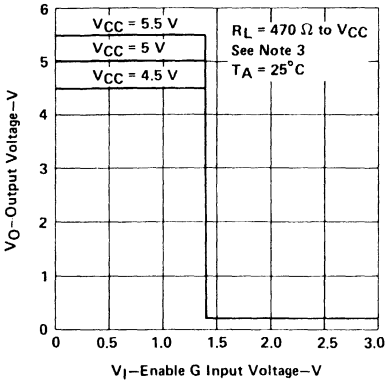


FIGURE 7

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

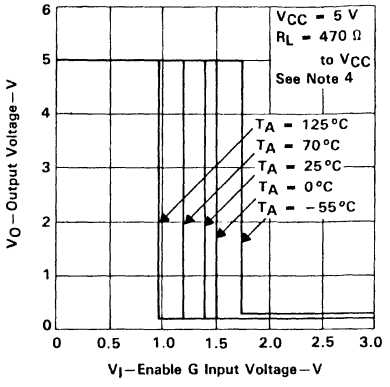


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

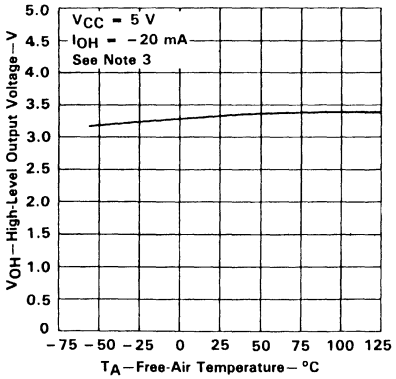


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

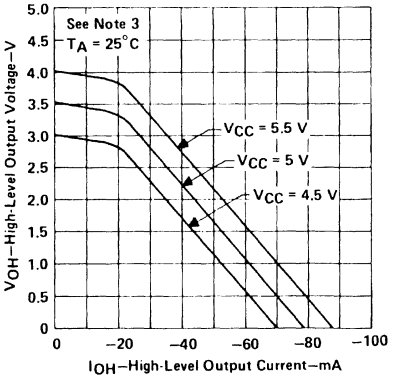


FIGURE 10

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

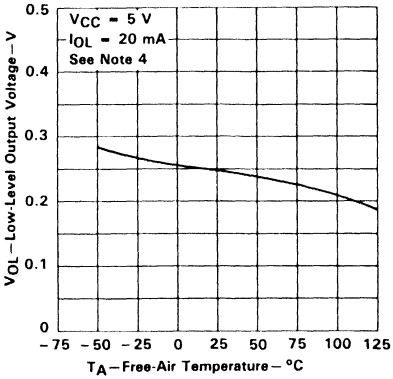


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

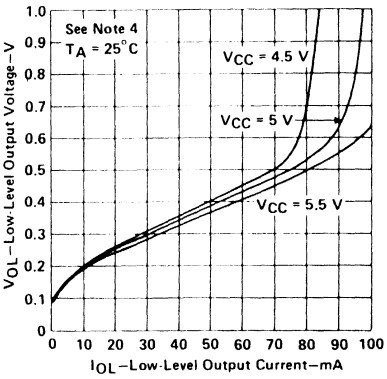


FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

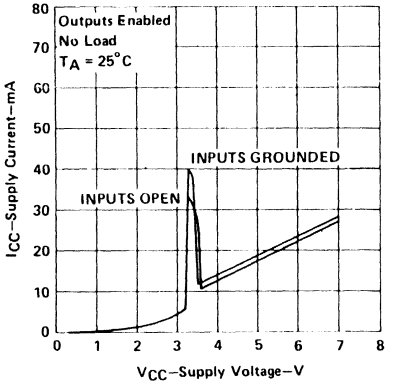


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

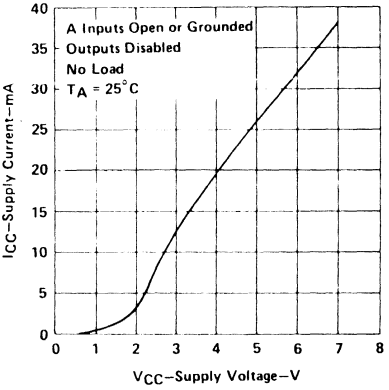


FIGURE 14

NOTE 4: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

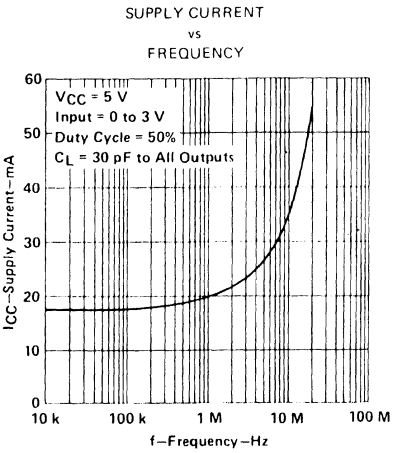
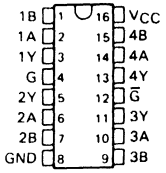


FIGURE 15

- Meets EIA Standards RS-422-A and RS-423-A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −7 V to 7 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-V Supply
- Low I_{CC} Requirements: I_{CC} . . . 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A

J PACKAGE
(TOP VIEW)



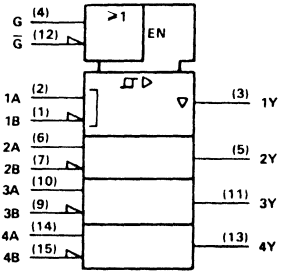
description

The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A and RS-423-A. It features 3-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 mV over a common-mode input voltage range of −7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

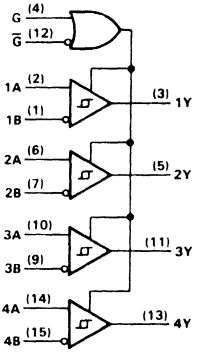
The SN75ALS193 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

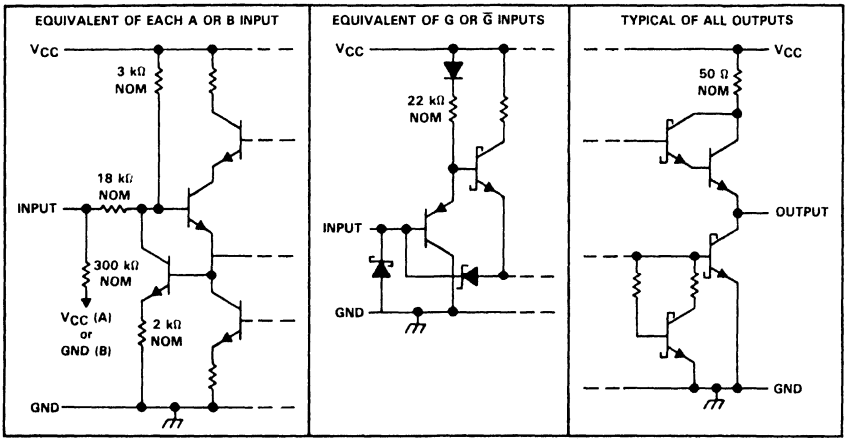


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1025 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200‡			mV
V_{hys}	Hysteresis§				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 1	I_{OH} = −400 μA,	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 3 V, See Note 5	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
5. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V, C_L = 15 pF,			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 2			15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		11	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		15	22	ns

PARAMETER MEASUREMENT INFORMATION

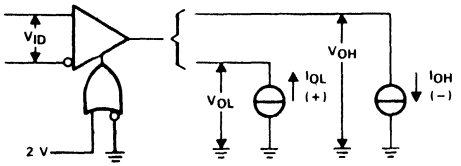
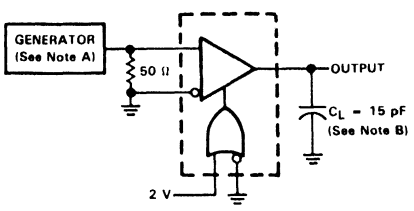
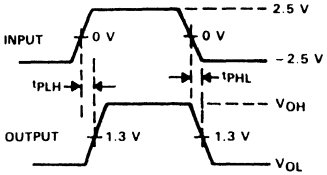


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

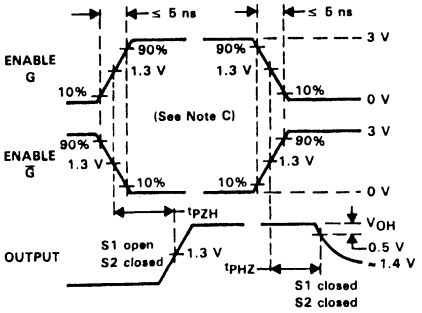


VOLTAGE WAVEFORMS

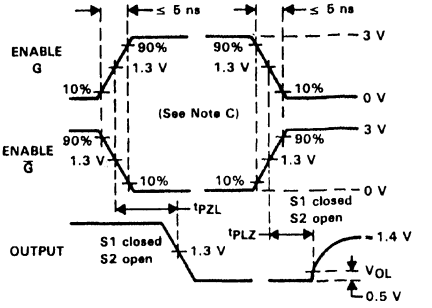
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}

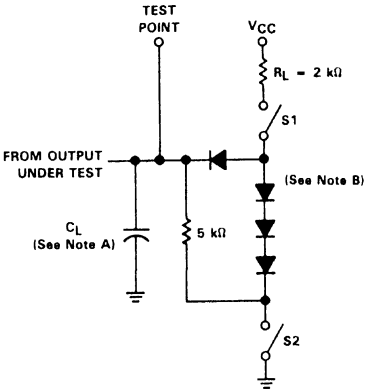
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}



LOAD CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 3. t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

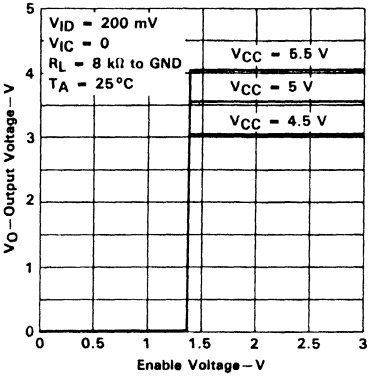


FIGURE 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

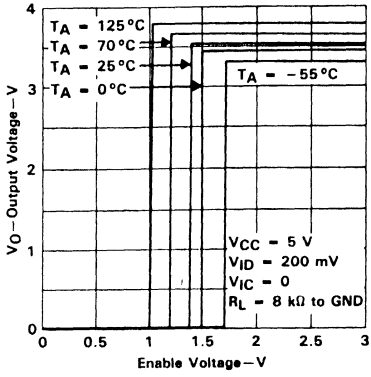


FIGURE 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

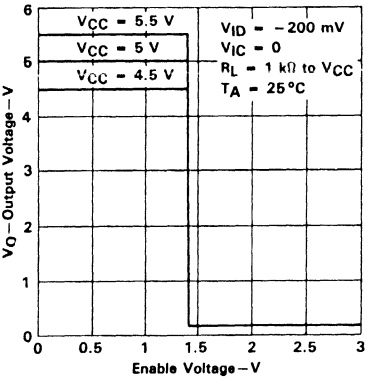


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

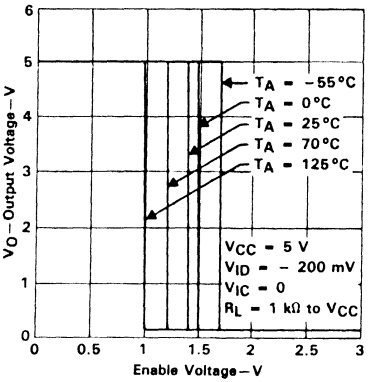


FIGURE 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

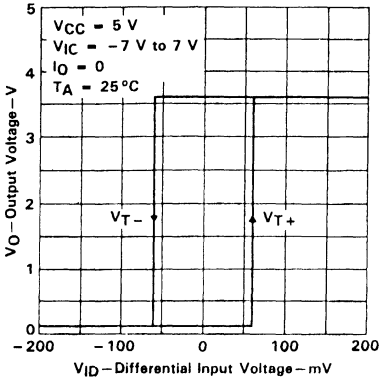


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

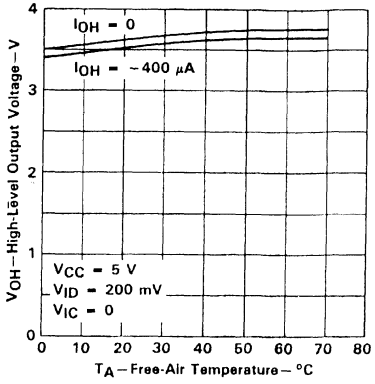


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

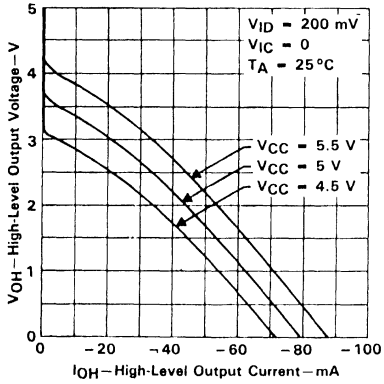


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

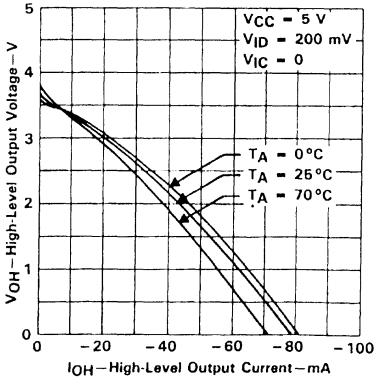


FIGURE 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

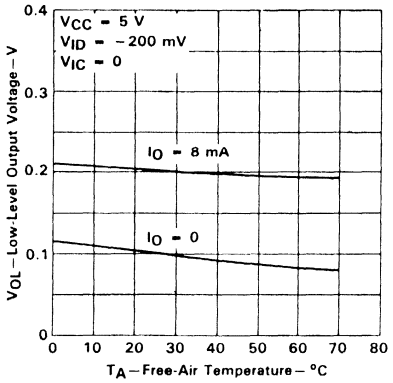


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

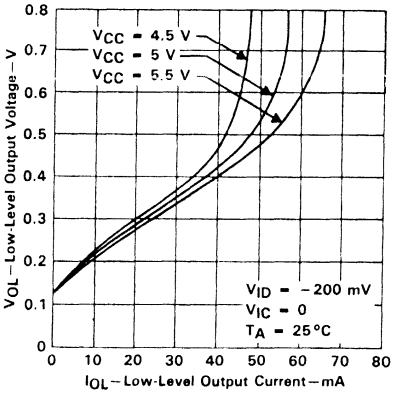


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

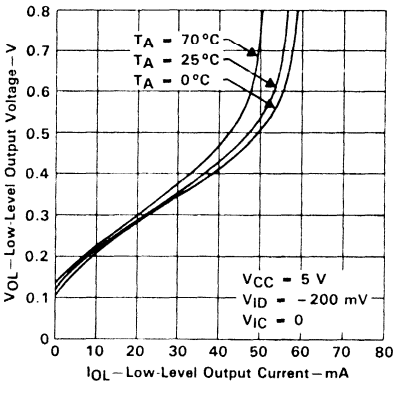


FIGURE 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

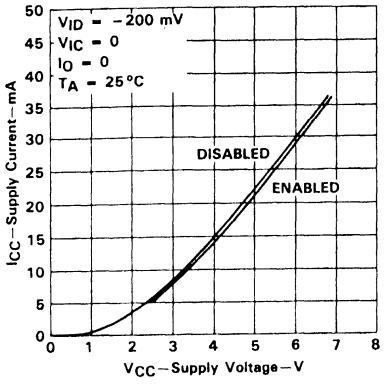


FIGURE 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

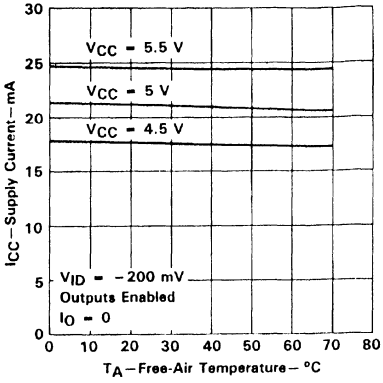


FIGURE 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

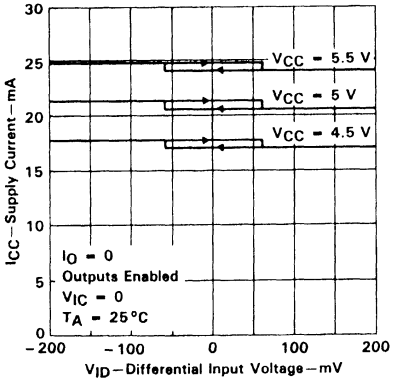


FIGURE 17

SUPPLY CURRENT
vs
FREQUENCY

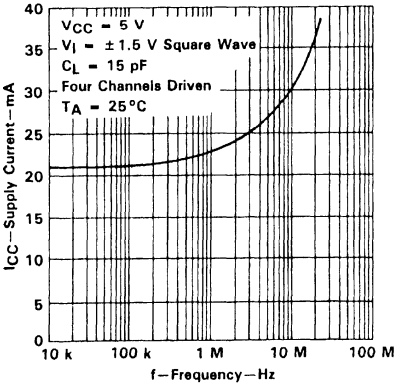


FIGURE 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

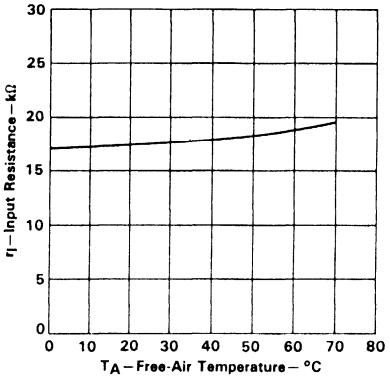


FIGURE 19

INPUT CURRENT
vs
INPUT VOLTAGE

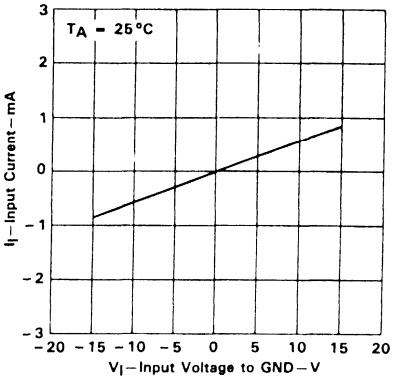


FIGURE 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

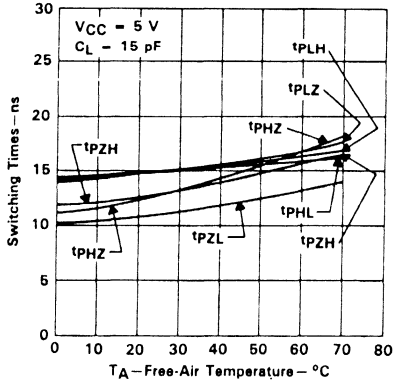


FIGURE 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

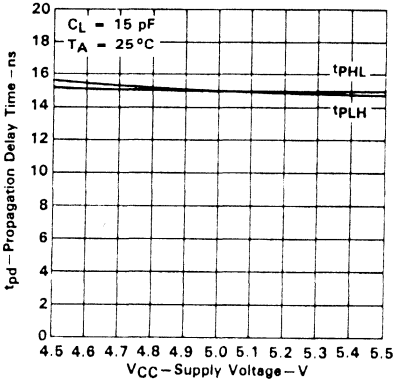


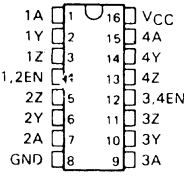
FIGURE 22

SN55ALS194, SN75ALS194
QUADRUPLE DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

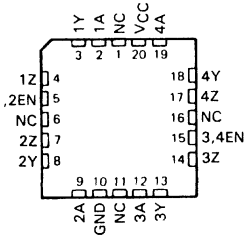
OCTOBER 1988

- **Meets EIA Standard RS-422-A**
- **High-Speed ALS Design**
- **3-State TTL-Compatible**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Two Pairs of Drivers Independently Enabled**
- **Designed as a Replacement for the MC3487 with Improvements: I_{CC} 50% Lower, Switching Speed 30% Faster, Full-Temperature-Range Version**

SN55ALS194 . . . J PACKAGE
SN75ALS194 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55ALS194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple complementary-output line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns and enable/disable times are typically less than 16 ns.

High-impedance inputs keep input currents low, less than 1 μA for a high level and less than 100 μA for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN55ALS194 and SN75ALS194 are capable of data rates in excess of 10 megabits per second and are designed to operate with the SN55ALS195 and SN75ALS195 quadruple line receivers.

The SN55ALS194 is characterized for operation from −55°C to 125°C. The SN75ALS194 is characterized for operation from 0°C to 70°C.

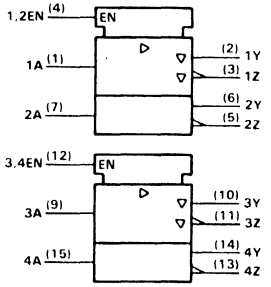
FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

H = TTL high level, L = TTL low level, X = irrelevant

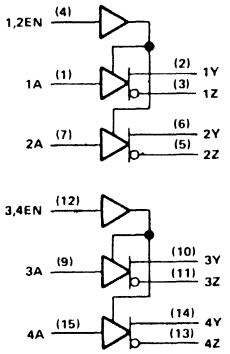
TEXAS INSTRUMENTS

logic symbol†

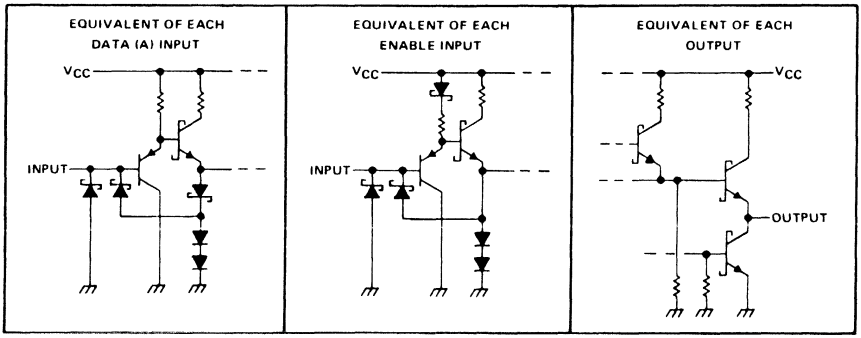


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55ALS194 . . . . . −55°C to 125°C
SN75ALS194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS194)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS194)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions

		SN55ALS194			SN75ALS194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	All inputs, T_A = 25°C	2			2			V
	A inputs, T_A = Full range	2			2			
	EN inputs, T_A = Full range	2.1			2			
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}				−20			−20	mA
Low-level output current, I_{OL}	T_A = 25°C			48			48	mA
	T_A = Full range			20			48	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −20 mA	SN55ALS194	2.4			V
			SN75ALS194	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX				0.5	V
VO	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		2		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			V
				2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance state output current	V_{CC} = MAX, Output enables at 0.8 V	V_O = 2.7 V			100	μA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			100	μA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−200	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_I = 2 V	−40		−140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX,	All outputs disabled		26	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55ALS194			SN75ALS194			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		6	13		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14		9	14	ns
	Output-to-output skew			3.5	6		3.5	6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 3		8	14		8	14	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 4		9	12		9	12	ns
t_{PZL}	Output enable time to low level			12	20		12	20	ns
t_{PHZ}	Output disable time from high level			9	15		9	14	ns
t_{PLZ}	Output disable time from low level			12	15		12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

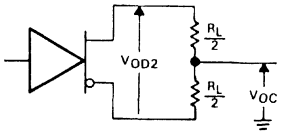


FIGURE 1. DRIVER V_{OD} AND V_{OC}

PARAMETER MEASUREMENT INFORMATION

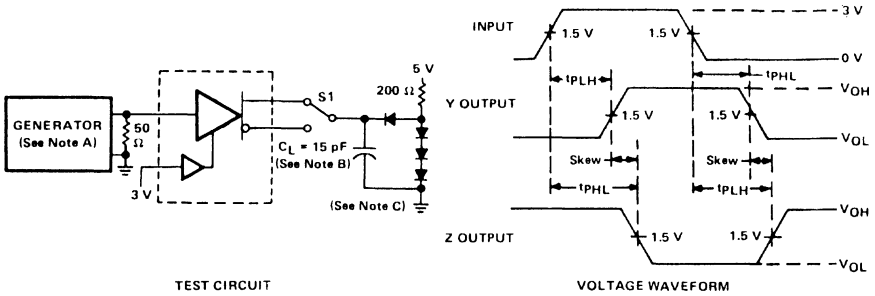


FIGURE 2. PROPAGATION DELAY TIMES

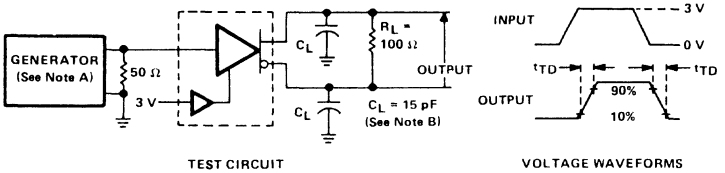
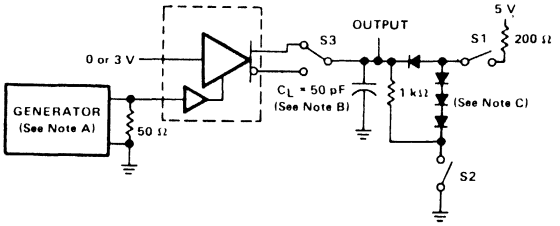


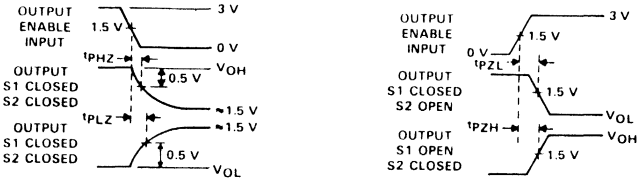
FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

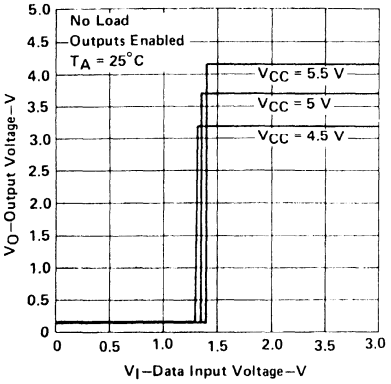


FIGURE 5

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

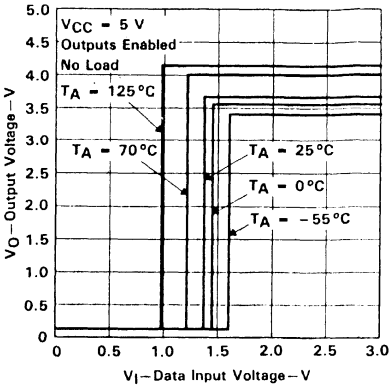


FIGURE 6

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

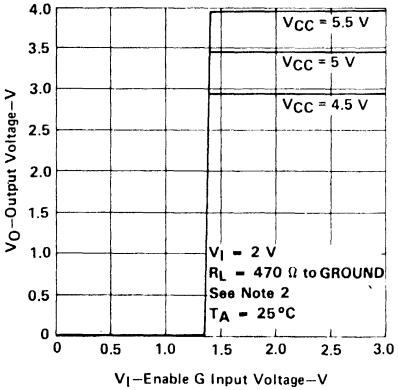


FIGURE 7

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

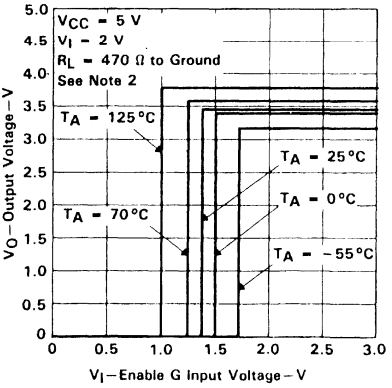


FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable to SN55ALS194 circuits only.
NOTE 2: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

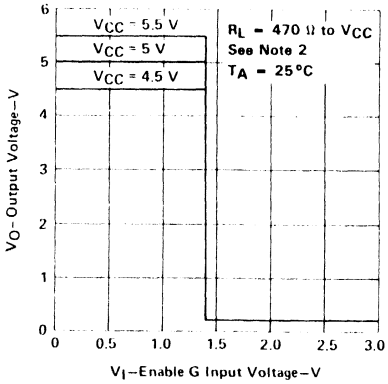


FIGURE 9

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

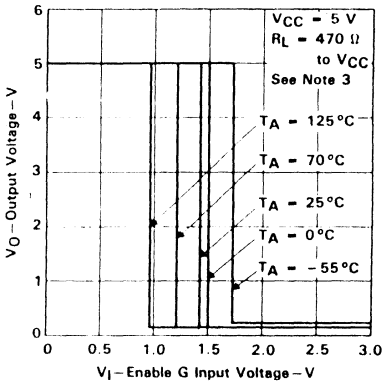


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

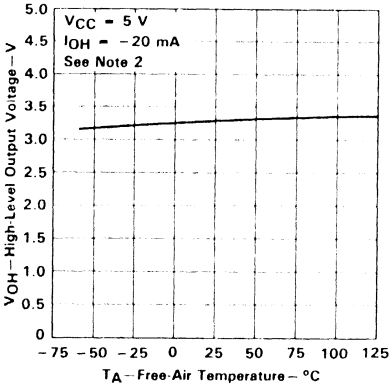


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

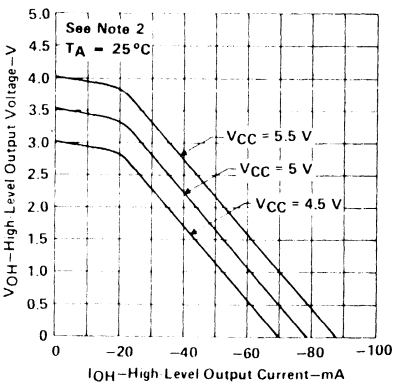


FIGURE 12

†Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
3 The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

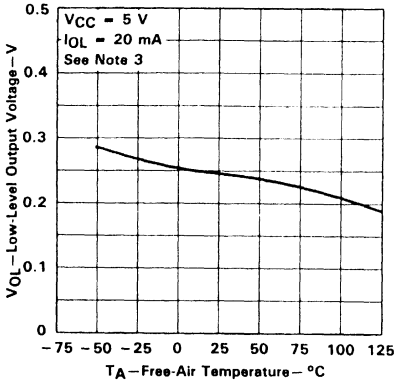


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

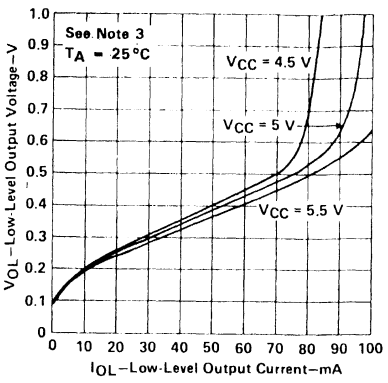


FIGURE 14

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

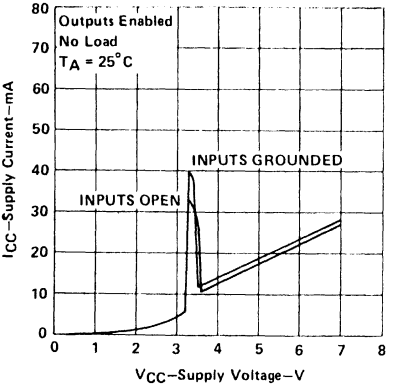


FIGURE 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

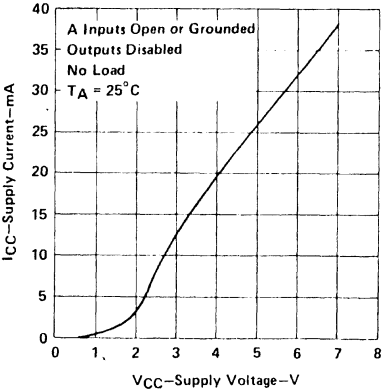


FIGURE 16

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.
NOTE 3: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

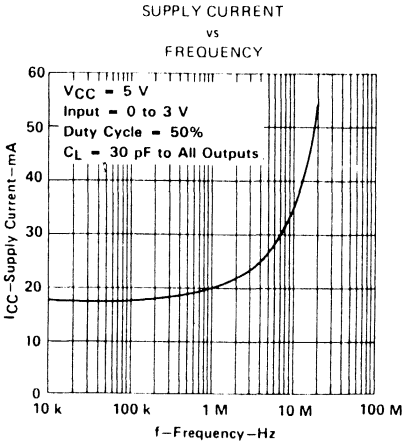


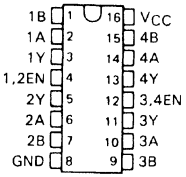
FIGURE 17

SN55ALS195, SN75ALS195
QUADRUPLE DIFFERENTIAL LINE RECEIVERS WITH 3-STATE OUTPUTS

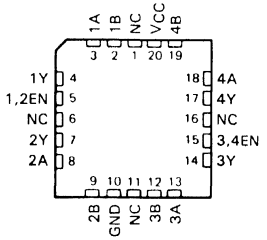
JUNE 1990

- Meets EIA Standards RS-422-A and RS-423-A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- −7 V to 7 V Common-Mode Range With 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 kΩ Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement . . . 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

SN55ALS195, SN75ALS195 . . . J PACKAGE
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

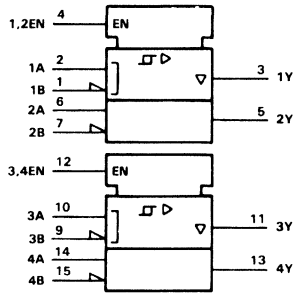
The SN55ALS195 and SN75ALS195 are monolithic quadruple line receivers with 3-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of EIA Standards RS-422-A and RS-423-A. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The devices are optimized for balanced multipoint bus transmission at rates up to 20M b/s. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 mV over a common-mode input voltage range of ±7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

The SN55ALS195 is characterized for operation from −55°C to 125°C. The SN75ALS195 is characterized for operation from 0°C to 70°C.

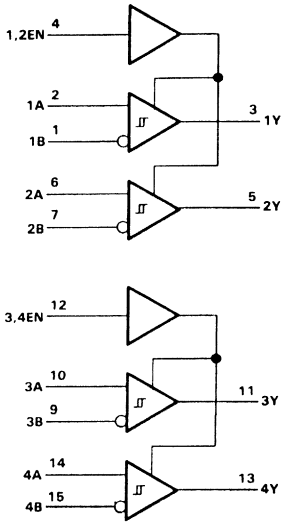
TEXAS INSTRUMENTS

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

logic diagram

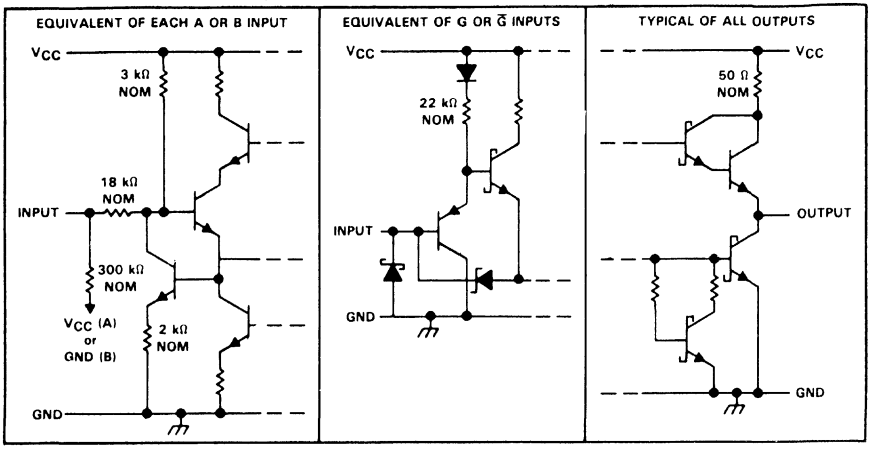


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A−B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} <$ 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level, L = low level, X = irrelevant,
? = indeterminate, and Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs, V_I . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55ALS195 . . . . . −55°C to 125°C
SN75ALS195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditons" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/°C	656 mW	N/A

recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Differential input voltage, V_{ID}			±12			±12	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200§			mV
V_{hys}	Hysteresis¶				120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} MIN, I_{OH} = −400 μA,	V_{ID} = 200 mV, See Figure 1	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance state output current	V_{CC} = MAX, V_{ID} = −3 V,	V_{IL} = 0.8 V, V_O = 2.7 V			20	μA
		V_{CC} = MAX, V_{ID} = −3 V,	V_{IL} = 0.8 V, V_O = 0.5 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_{CC} = MIN, V_I = 15 V		0.7	1.2	mA
			V_{CC} = MAX, V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0,	V_{ID} = 3 V, See Note 4	−15	−78	−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled		22	35	mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
¶Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTES: 3. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
4. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 V to 3 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				10	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		19	25	ns
t_{PLZ}	Output disable time from low level				17	22	

PARAMETER MEASUREMENT INFORMATION

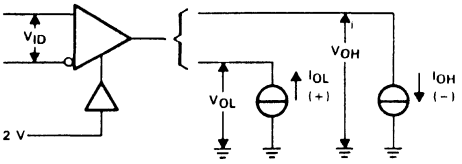
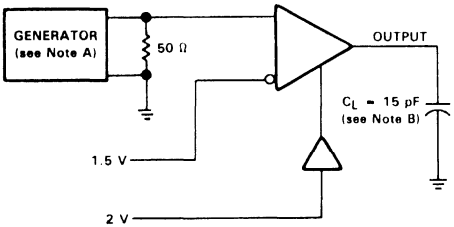
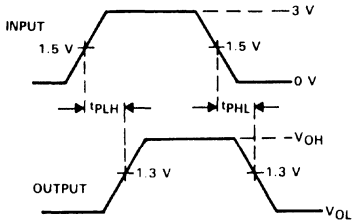


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

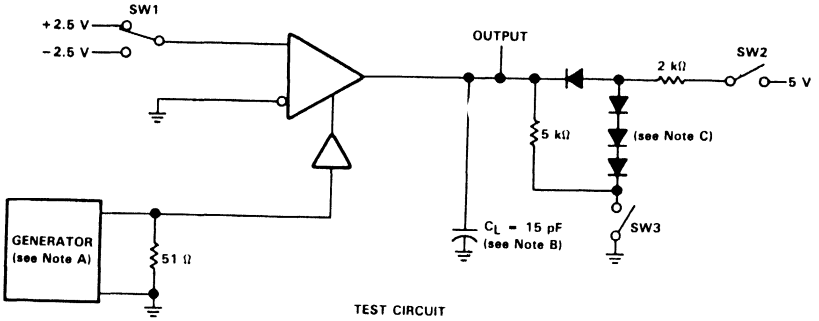


VOLTAGE WAVEFORMS

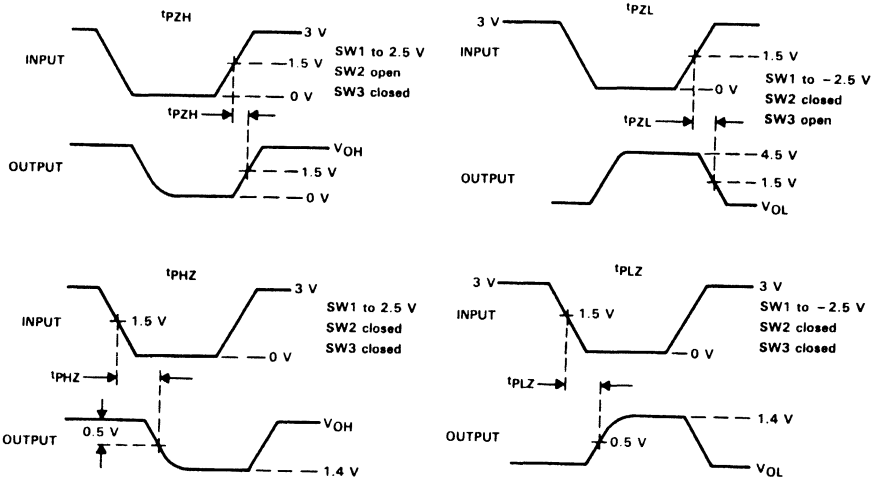
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 3. ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

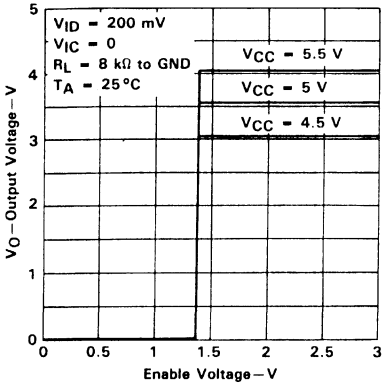


FIGURE 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

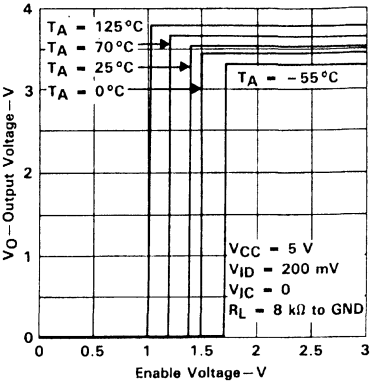


FIGURE 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

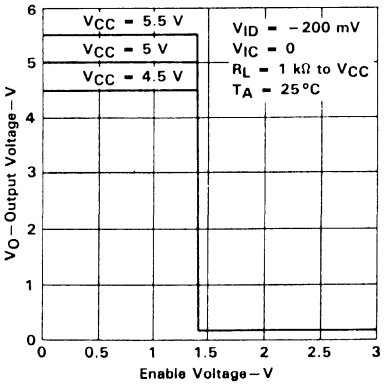


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

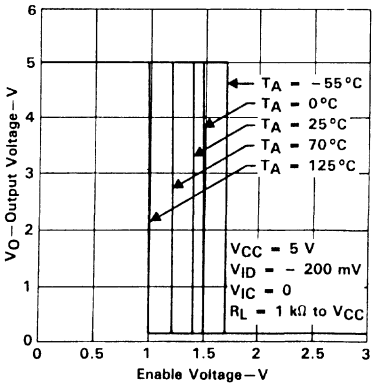


FIGURE 7

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

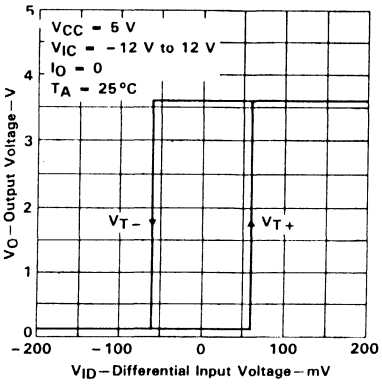


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

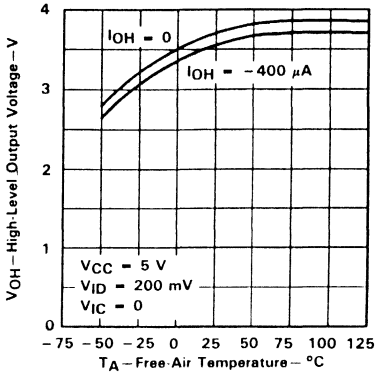


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

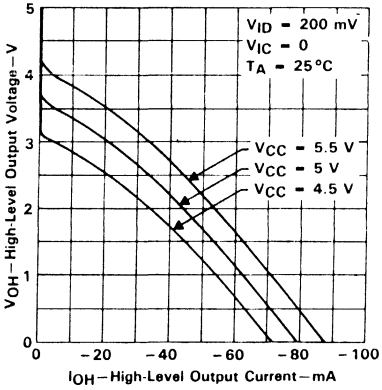


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

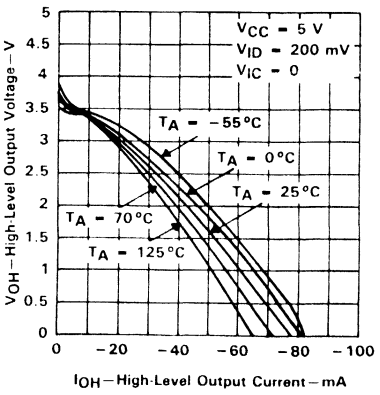


FIGURE 11

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

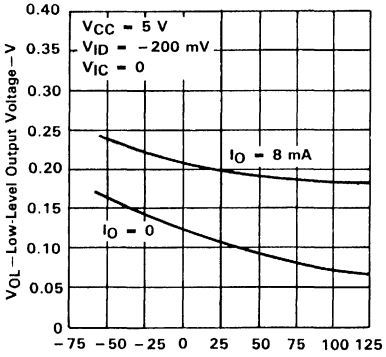


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

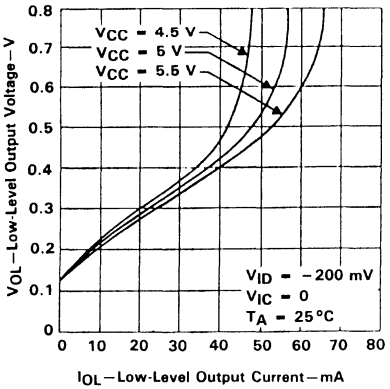


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

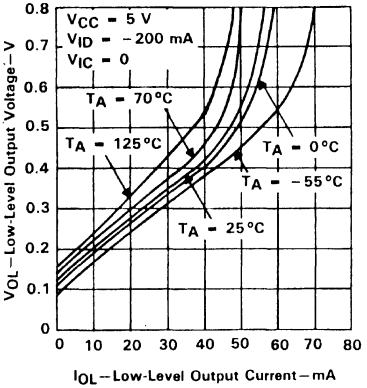


FIGURE 14

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

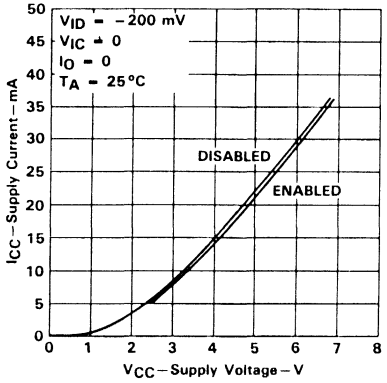


FIGURE 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

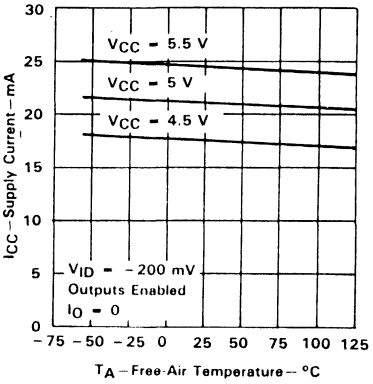


FIGURE 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

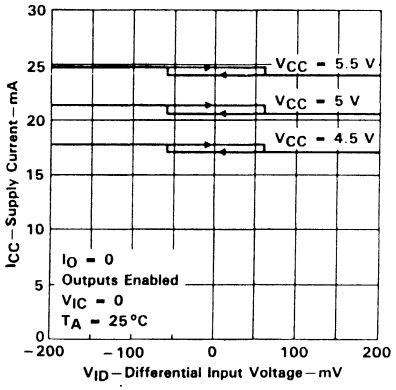


FIGURE 17

SUPPLY CURRENT
vs
FREQUENCY

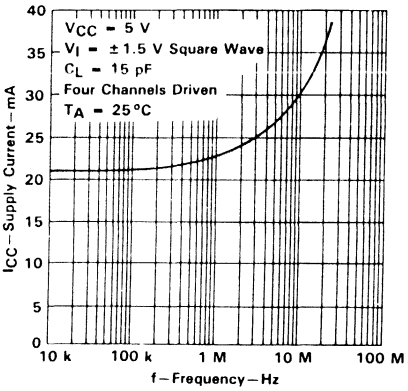


FIGURE 18

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

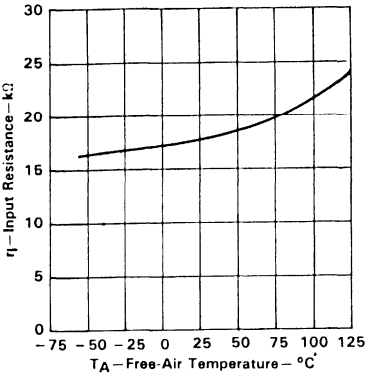


FIGURE 19

INPUT CURRENT
vs
INPUT VOLTAGE

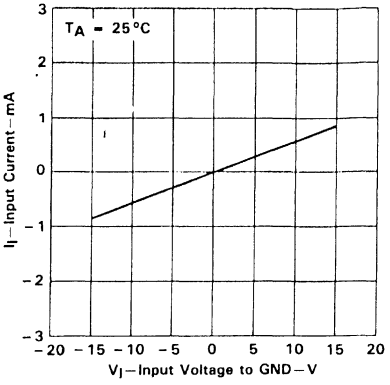


FIGURE 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

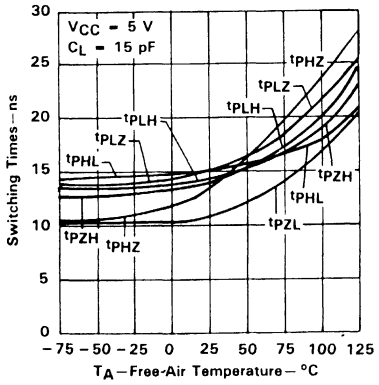


FIGURE 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

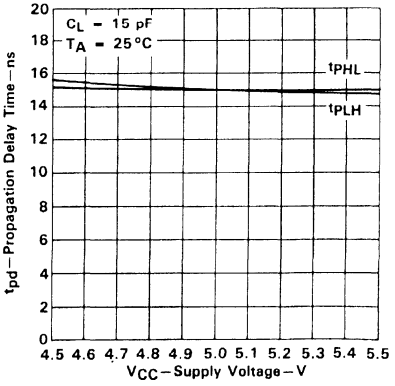


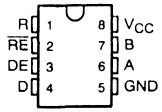
FIGURE 22

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TEXAS INSTRUMENTS

- Bidirectional Transceiver
- Meets EIA Standard RS-485 and ISO 8482:1987(E)
- High-Speed Low-Power LinBICMOS™ Circuitry
- Designed for High-Speed Operation In Both Serial and Parallel Applications
- Low Skew
- Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments
- Very Low Disabled Supply Current Requirements . . . 200 μA Maximum
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Open Circuit Fail-Safe Receiver Design
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A–B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

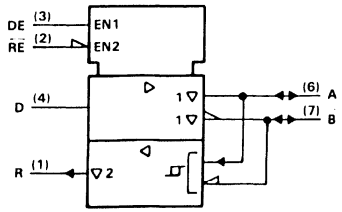
The SN65LBC176 and SN75LBC176 differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standard RS-485 and ISO 8482:1987(E).

The SN65LBC176 and SN75LBC176 combine a 3-state differential-line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party line applications. Very low device supply current can be acheived by disabling the driver and the receiver. Both the driver and receiver are available as cells in the Texas Instruments LinASIC™ Library.

The SN65LBC176 is characterized for operation from −40°C to 85°C and the SN75LBC176 is characterized for operation from 0°C to 70°C.

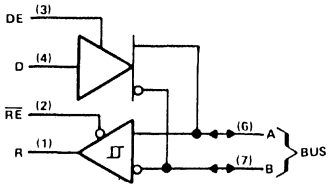
LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†

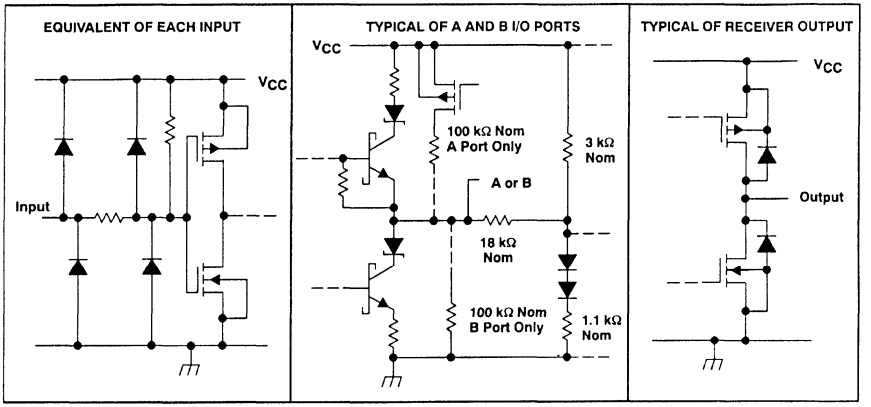


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC176 ..... −40°C to 85°C
SN75LBC176 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65LBC176	−40		85	°C
	SN75LBC176	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA					−1.5	V
V_O	Output voltage	$I_O = 0$			0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$			1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 54\ \Omega$,	See Figure 1	75LBC176	1.5	2.25	5	V
				65LBC176	1.3			
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	75LCB176	1.5		5	V
				65LBC176	1.3			
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$ or $100\ \Omega$, See Figure 1					±0.2	V
V_{OC}	Common-mode output voltage						3	V
							−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage‡						±0.2	V
I_O	Output current	Output disabled, See Note 3	$V_O = 12$ V				1	mA
			$V_O = -7$ V				−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V					20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V					−100	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V					−250	mA
		$V_O = 0$					−150	
		$V_O = V_{CC}$					250	
		$V_O = 12$ V						
I_{CC}	Supply current	$V_I = 0$ or V_{CC}, No load	Receiver disabled and driver enabled				1500	μA
			Receiver and driver disabled				200	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions.

driver switching characteristics over recommended ranges of supply voltage, $T_A = 0°C$ to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	$R_L = 54\ \Omega$, $C_L = 50$ pF, See Figure 3	8		25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{DDH} - t_{DDL} \rvert$)			0	6	ns
t_{PLH}	Propagation time, low-to-high-level single-ended output				26	ns
t_{PHL}	Propagation time, high-to-low-level single-ended output				26	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4			60	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$, See Figure 5			60	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$, See Figure 4			60	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$, See Figure 5			60	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	V_t (Test Termination Measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	
I_O	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled			3.9	mA
			Receiver and driver disabled			200	μA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	20		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output		28		45	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			10	18	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8			30	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 8			30	ns
t_{PLZ}	Output disable time from low level				30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

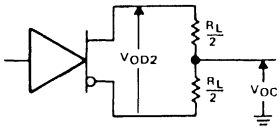


Figure 1. Driver V_{OD} and V_{OC}

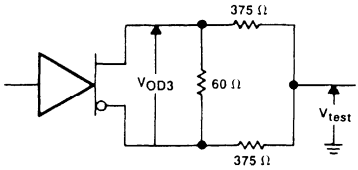


Figure 2. Driver V_{OD3}

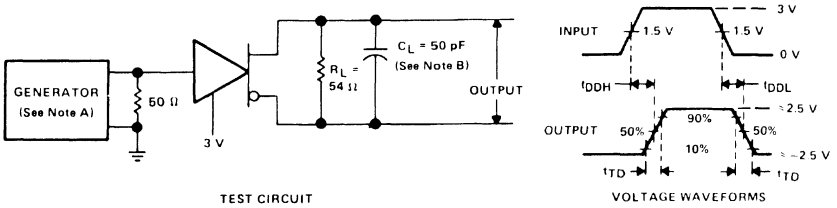


Figure 3. Driver Differential-Output Delay and Transition Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

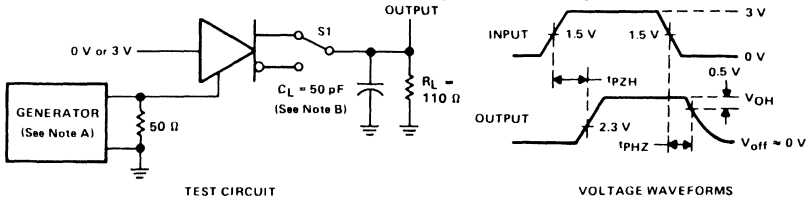


Figure 4. Driver Enable and Disable Times

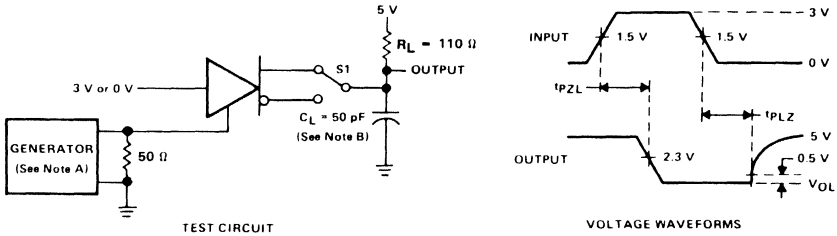


Figure 5. Driver Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

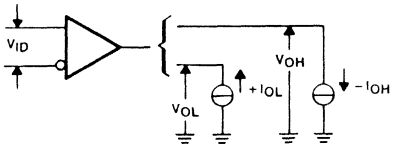


Figure 6. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

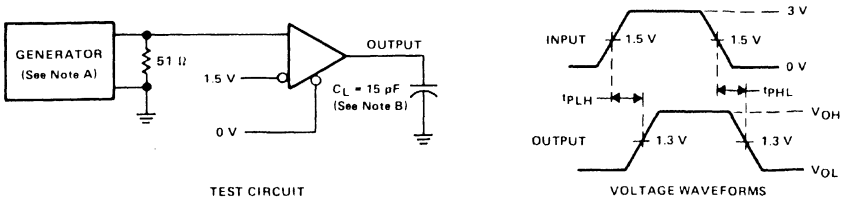


Figure 7. Receiver Propagation Delay Times

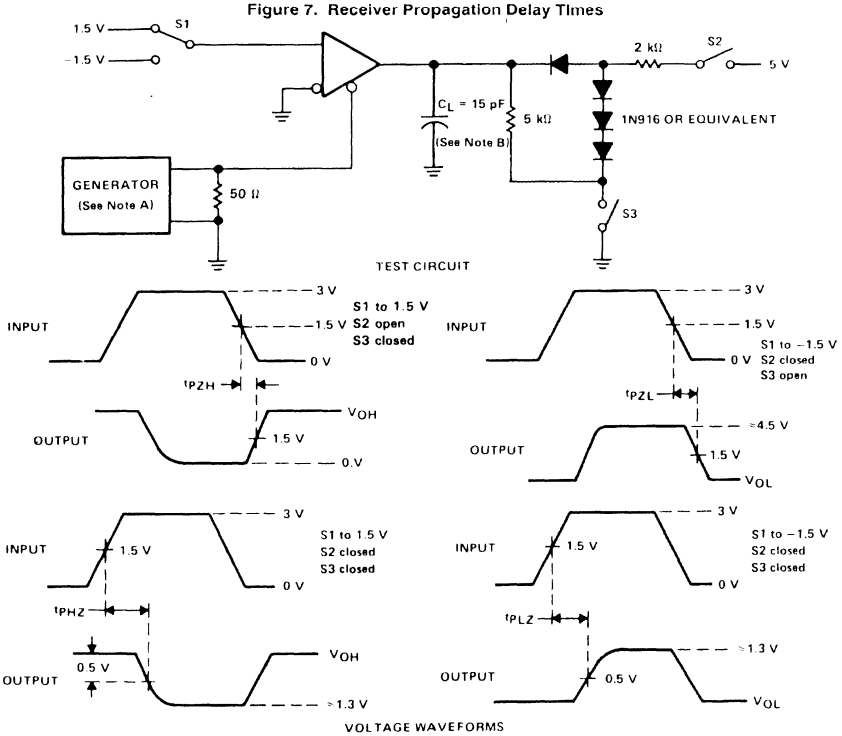
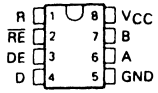


Figure 8. Receiver Output Enable and Disable Times

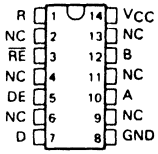
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

- Bidirectional Transceiver
- Suitable for Most EIA Standards RS-422-A and RS-485 Applications
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

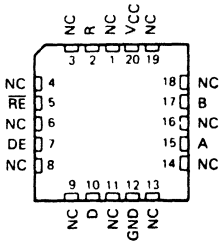
JG PACKAGE
(TOP VIEW)



W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN95176B differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. These transceivers are suitable for most RS-422-A and RS-485 applications to the extent of the specified data sheet characteristics and operating conditions.

The SN95176B combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

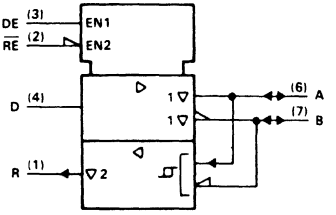
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description (continued)

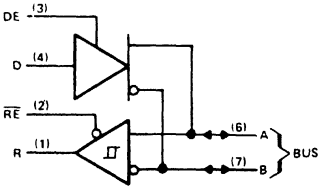
The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN95176B is characterized for operation from −40°C to 110°C.

logic symbol†

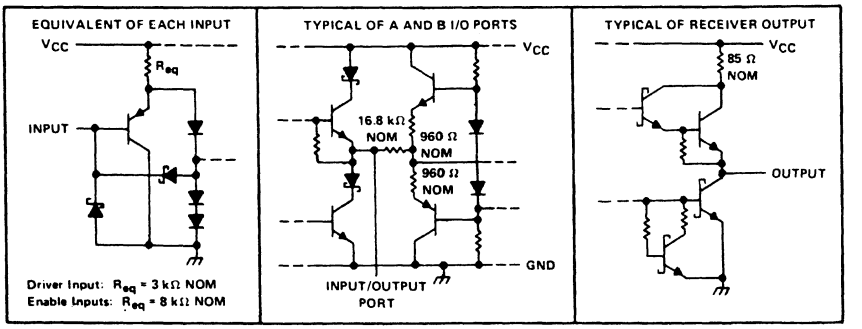


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JG package.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −40°C to 110°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: JG or W package . . . . 300°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 110°C POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	336 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	320 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		−40		110	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 3			4		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Outputs disabled,	V_O = 12 V			1	mA
		See Note 4	V_O = −7 V			−0.8	mA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	mA
		V_O = V_{CC}				250	mA
		V_O = 12 V				250	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	mA

†The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
4. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{TD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V,			21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

PARAMETER MEASUREMENT INFORMATION

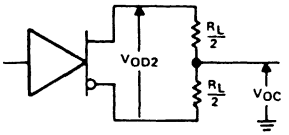


FIGURE 1. DRIVER V_{OD} AND V_{OC}

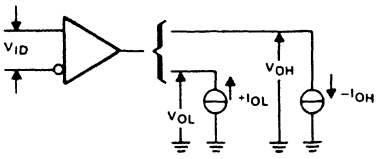


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

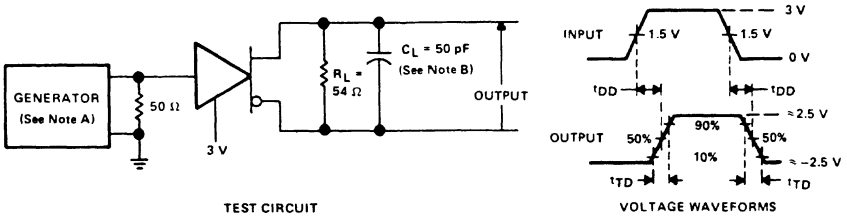


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

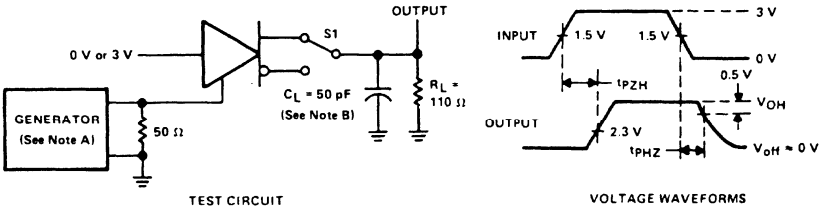


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

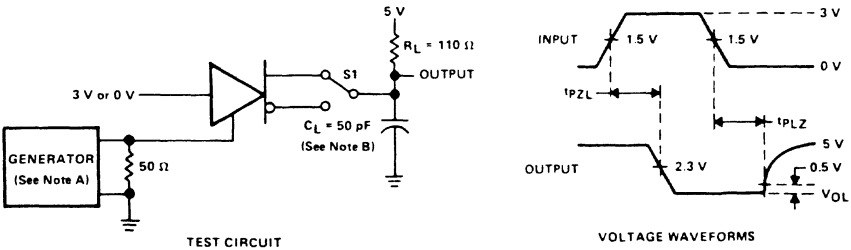


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Equivalent test circuits may be substituted for actual testing.

PARAMETER MEASUREMENT INFORMATION

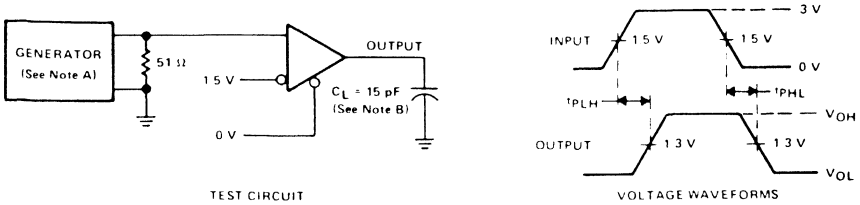


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

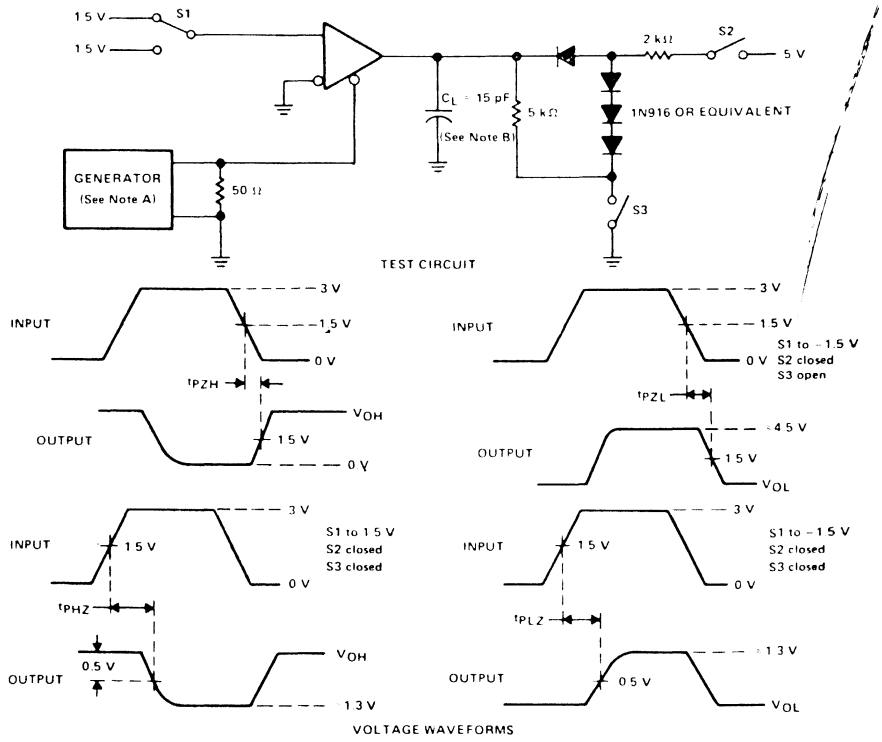


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 5 ns, Z_O ≈ 50 Ω.

B. C_L includes probe and jig capacitance.

C. Equivalent test circuits may be substituted for actual testing.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

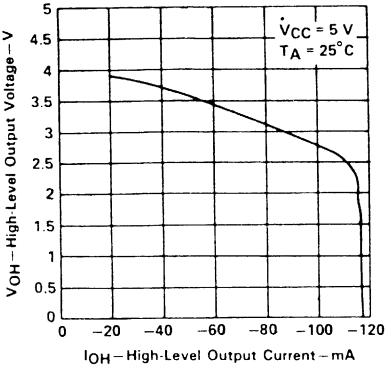


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

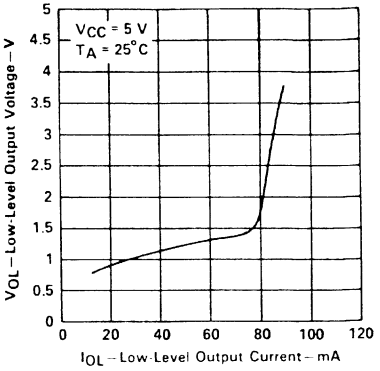


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

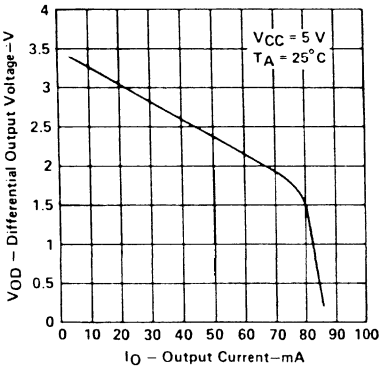


FIGURE 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

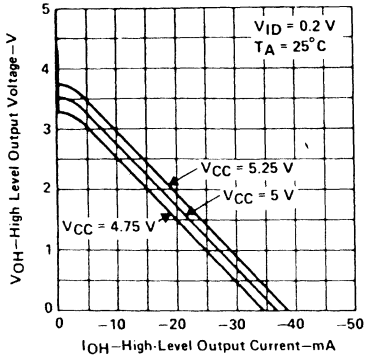


FIGURE 11

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

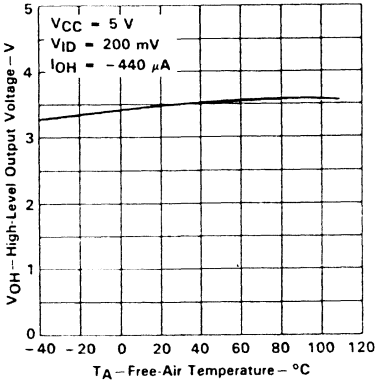


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

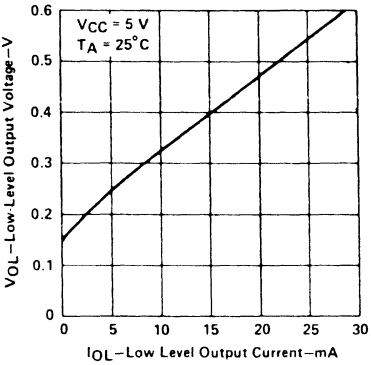


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

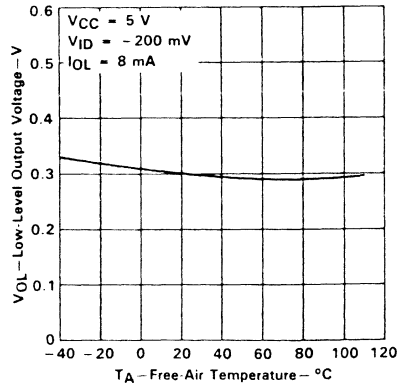


FIGURE 14

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

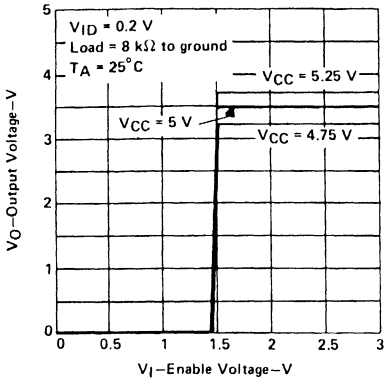


FIGURE 15

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

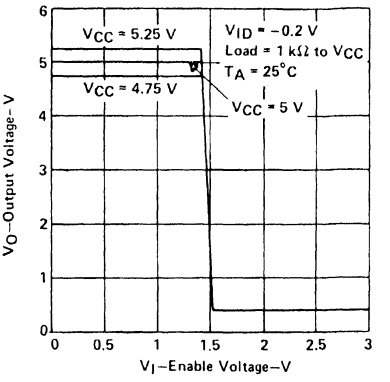
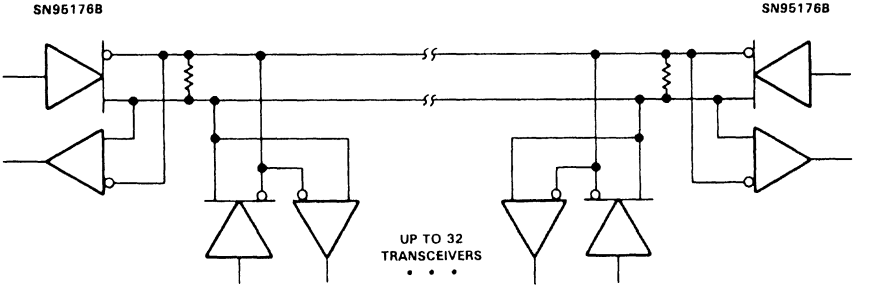


FIGURE 16

APPLICATION INFORMATION



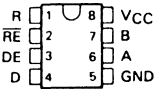
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 17. TYPICAL APPLICATION CIRCUIT

TEXAS INSTRUMENTS

- **Bidirectional Transceiver**
- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation In Both Serial and Parallel Applications**
- **Low Skew . . . 8 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments**
- **Low Supply Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 70 mV Typ**
- **Fail Safe . . . High Receiver Output with Inputs Open**
- **Operates from a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Interchangeable with National DS3695**

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

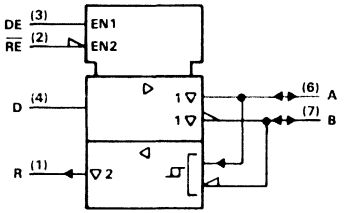
INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs Open	L	H

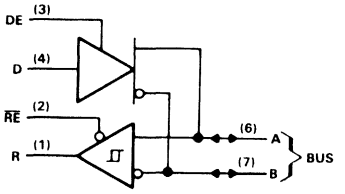
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

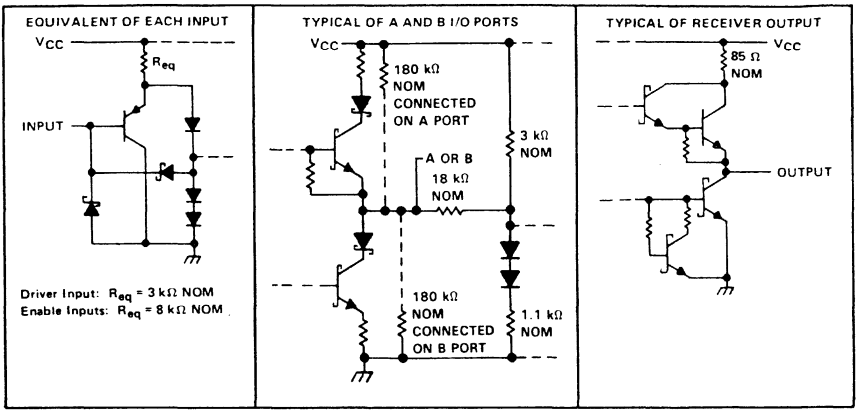
The TL3695 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The TL3695 combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs

and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		5	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	µA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	$C_{L1} = C_{L2} = 100$ pF,	$R_L = 60\ \Omega$,	See Figure 3		8	22	ns
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)					1	8	ns
t_{TD}	Differential output transition time					8	18	ns
t_{PZH}	Output enable time to high level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 4			50	ns
t_{PZL}	Output enable time to low level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 5			50	ns
t_{PHZ}	Output disable time from high level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 4		8	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 5		8	30	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	V_{os}
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§	V_{OC} = 0			70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV or Inputs open I_{OH} = −400 μA,	See Figure 6	2.4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 16 mA			0.5	V
		See Figure 6	I_{OL} = 8 mA			0.45	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_O = 0		−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,	C_L = 15 pF,		14	37	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 7			14	37	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 8		7	20	ns
t_{PZL}	Output enable time to low level				7	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 8		7	16	ns
t_{PLZ}	Output disable time from low level				8	16	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

PARAMETER MEASUREMENT INFORMATION

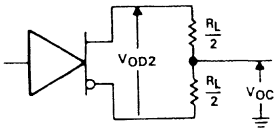


FIGURE 1. DRIVER V_{OD} AND V_{OC}

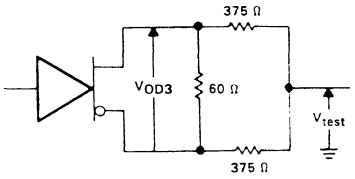
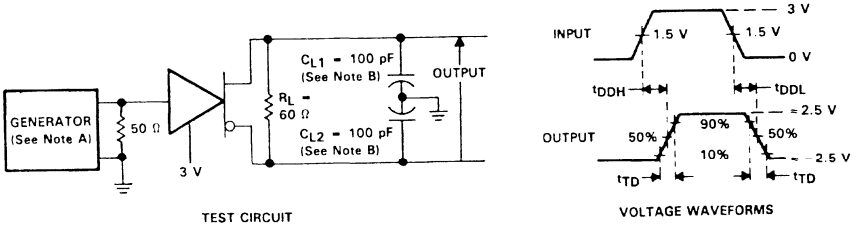
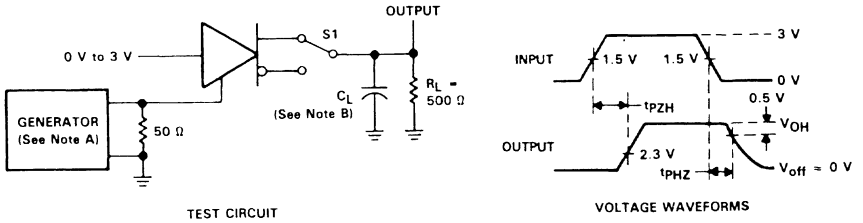


FIGURE 2. DRIVER V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

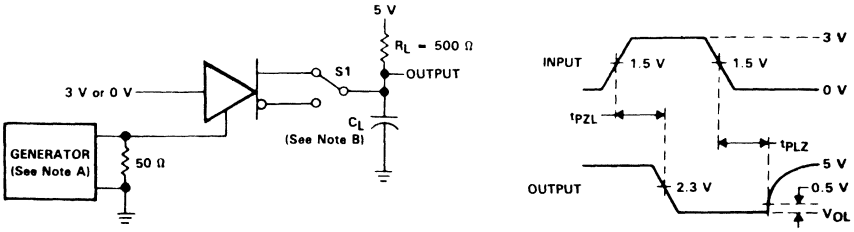
FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance. (See switching characteristics – test conditions)

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance. (See switching characteristics – test conditions)

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

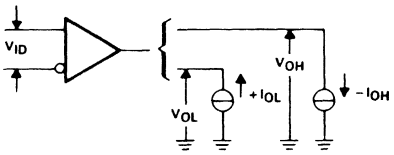
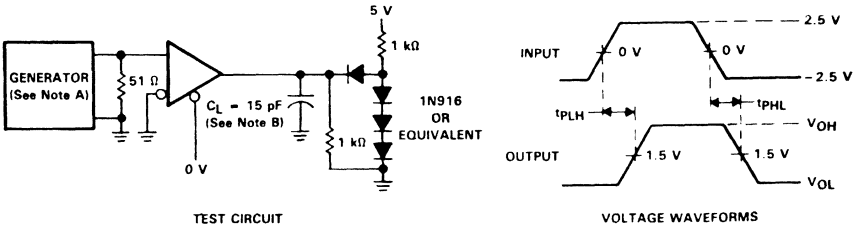


FIGURE 6. RECEIVER V_{OH} AND V_{OL}

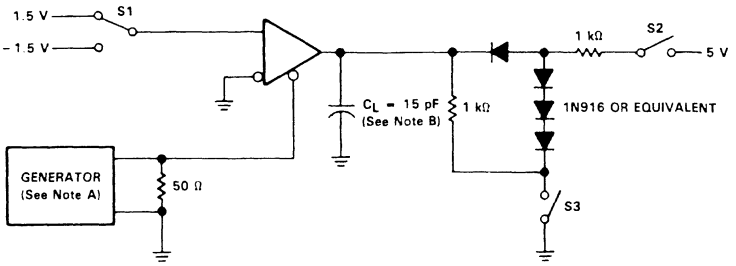


TEST CIRCUIT VOLTAGE WAVEFORMS

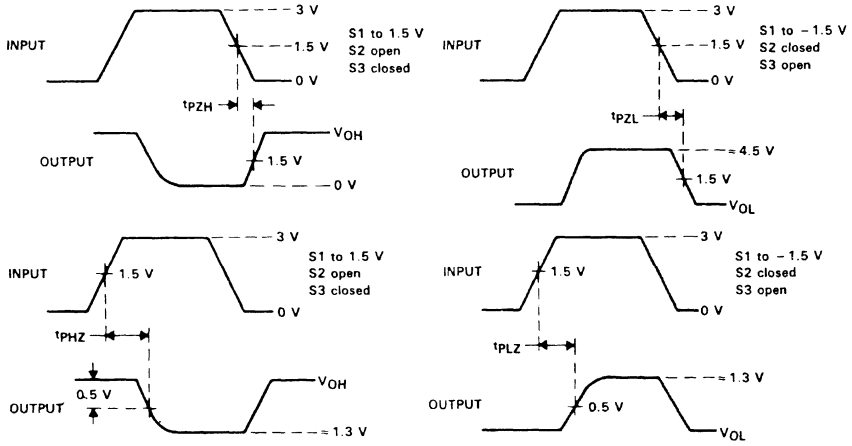
NOTES: A. The input pulse is supplied by.a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

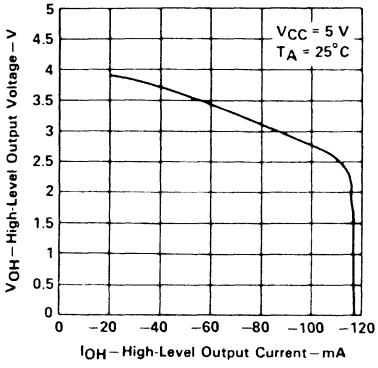


FIGURE 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

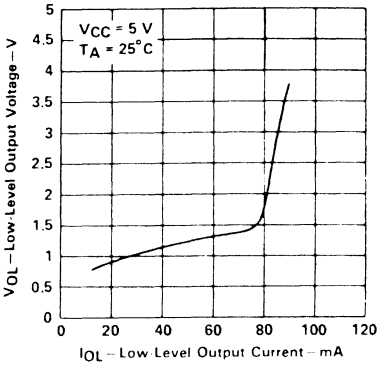


FIGURE 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

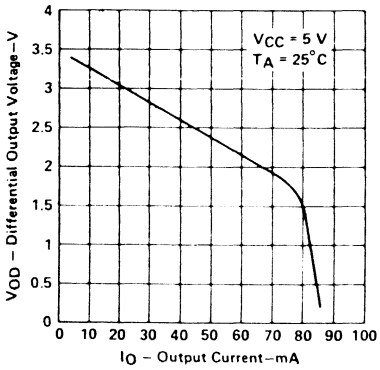


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

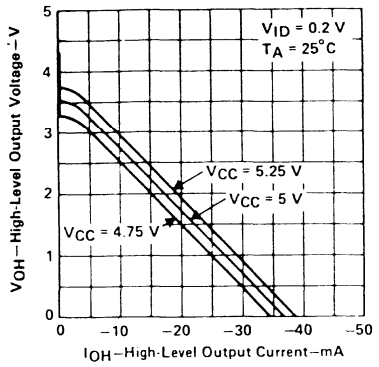


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

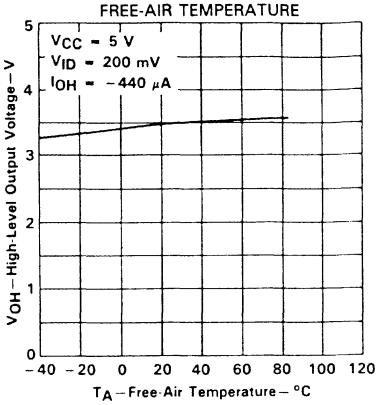


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

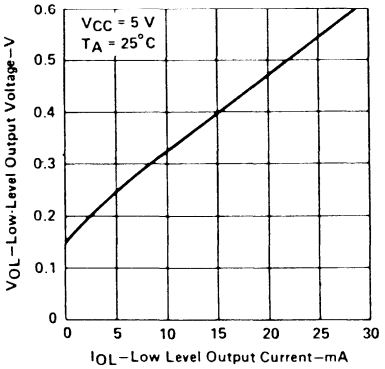


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

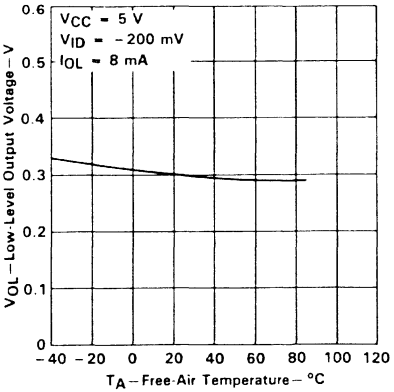


FIGURE 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

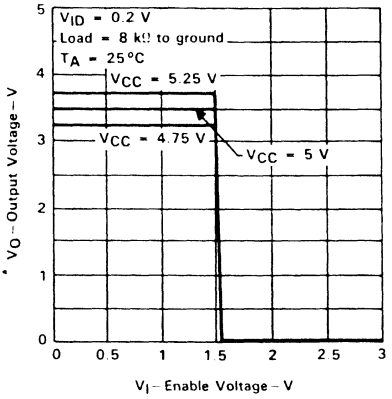


FIGURE 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

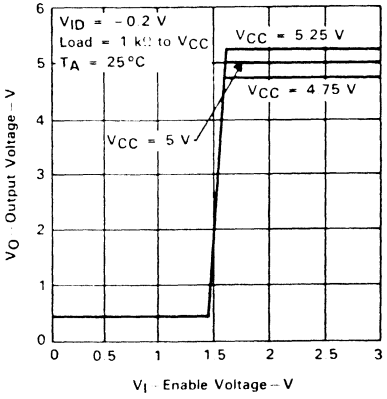
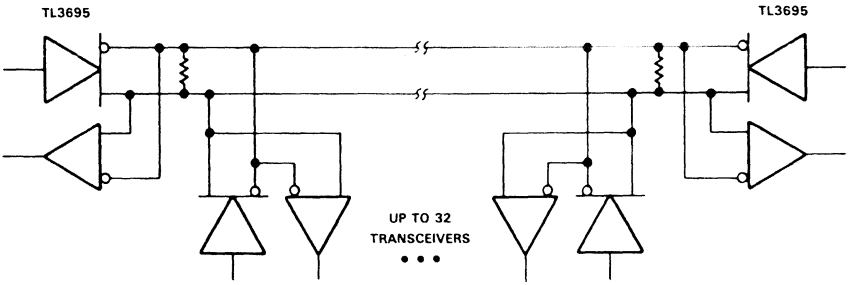


FIGURE 17

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

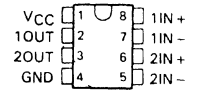
FIGURE 18. TYPICAL APPLICATION CIRCUIT

uA9637, uA9637AC
DUAL DIFFERENTIAL LINE RECEIVER

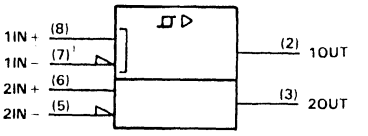
NOVEMBER 1986

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets Federal Standards 1020 and 1030**
- **Operates from Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line and "Small Outline" Packages**
- **Similar to SN75157 except for Corner V_{CC} and Ground Pin Positions**
- **Designed to Be Interchangeable with Fairchild μA9637A**

uA9637M . . . JG PACKAGE
uA9637C . . . D, JG, OR P PACKAGE
(TOP VIEW)



logic symbol†



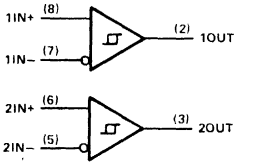
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

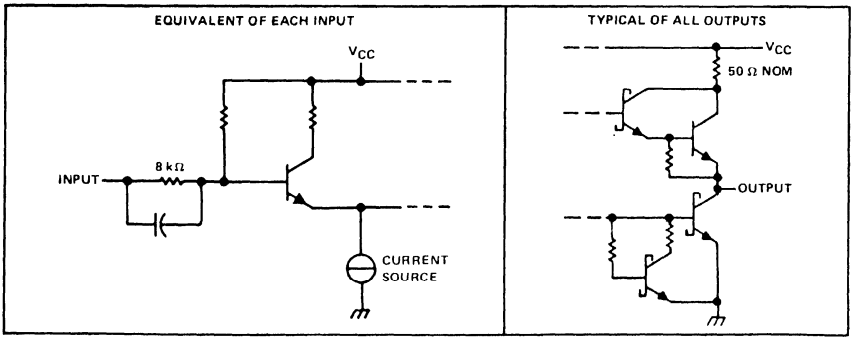
The uA9637AC is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and small outline package.

The uA9637AM is characterized over the full military temperature range of −55 °C to 125 °C. The uA9637AC is characterized for operation from 0 °C to 70 °C.

logic diagram



schematics of inputs and outputs



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package: uA9637AM . . . . . 1050 mW
uA9637AC . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range: uA9637AM . . . . . −55°C to 125°C
uA9637AC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate linearly at the following rates: 5.8 mW/°C for the D package, 8.4 mW/°C for uA9637AM in the JG package, 6.6 mW/°C for uA9637AC in the JG package, and 8.0 mW/°C for the P package.

recommended operating conditions

	uA9637AM			uA9637AC			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

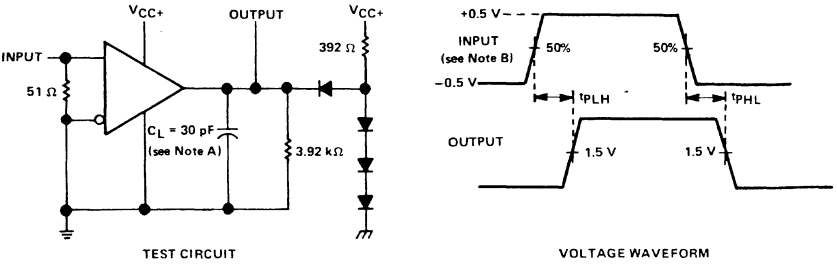
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
				See Note 4			
V_T	Threshold voltage (V_{T+} and V_{T-})	See Note 5		−0.2		0.2	V
				−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 4. The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

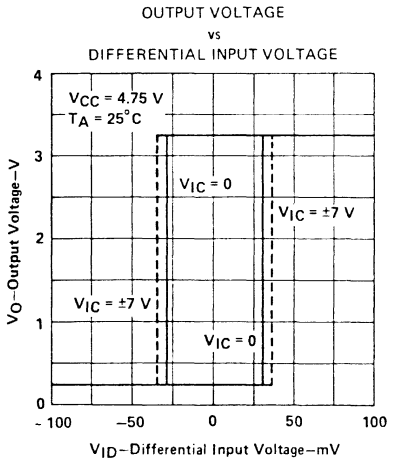


FIGURE 2

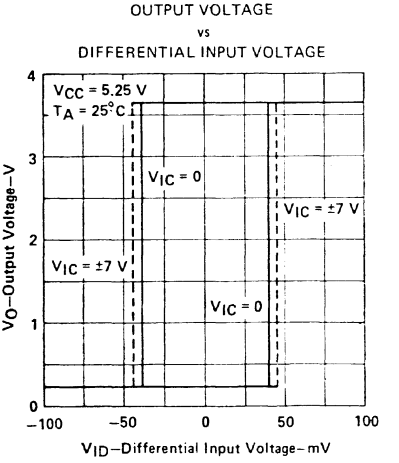


FIGURE 3

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

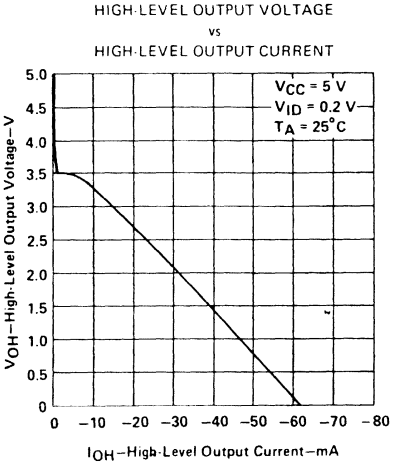


FIGURE 4

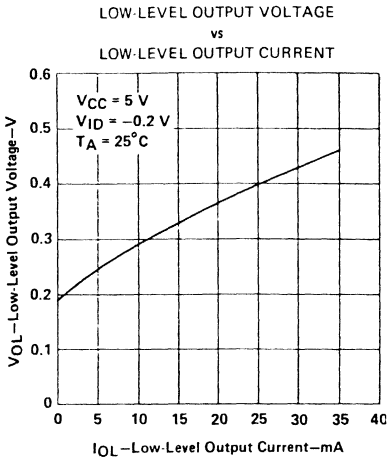


FIGURE 5

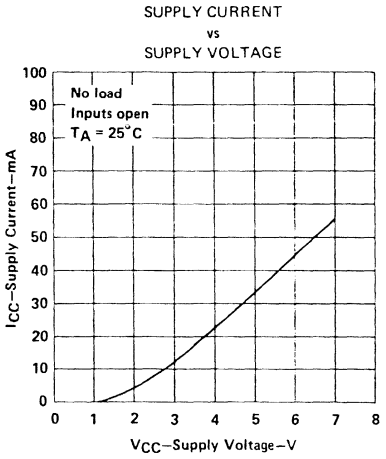


FIGURE 6

TYPICAL APPLICATION DATA

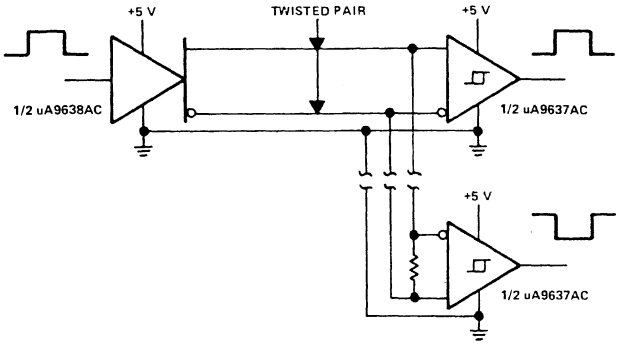
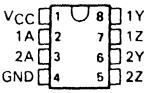


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

- **Meets EIA Standard RS-422-A**
- **Operates From a Single 5-V Supply**
- **TTL-and CMOS-Input Compatibility**
- **Output Short-Circuit Protection**
- **Schottky Circuitry**
- **Designed to Be Interchangeable With Fairchild 9638**

D, JG, OR P PACKAGE
(TOP VIEW)

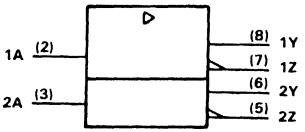


description

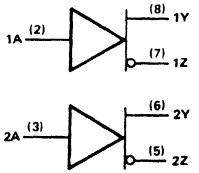
The uA9638C is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

The uA9638C is characterized for operation from 0°C to 70°C.

logic symbol†



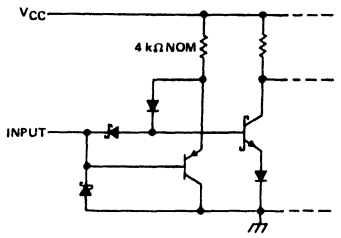
logic diagram



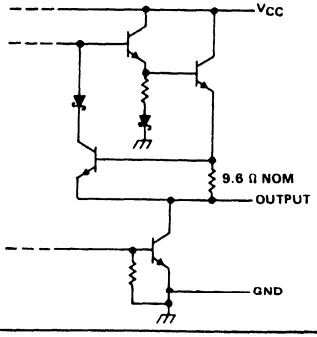
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range . . . . . −0.5 V to 7 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from 10 seconds: D and P package . . . . . 260°C

NOTES: 1. Voltage values except differential output voltages are with respect to network ground terminal.
2. In the JG package, uA9638C chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 1		2			V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of‡ differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of‡ common-mode output voltage					±0.4	V
I_O	Output current with power off	V_{CC} = 0,	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0		−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, No load,	All inputs at 0 V		45	65	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶Only one output at a time should be shorted and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		10	15	ns
t_{TD}	Differential-output transition time			10	15	ns
	Skew			1		ns

PARAMETER MEASUREMENT INFORMATION

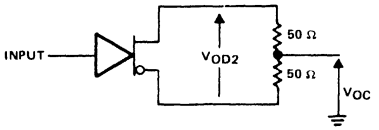
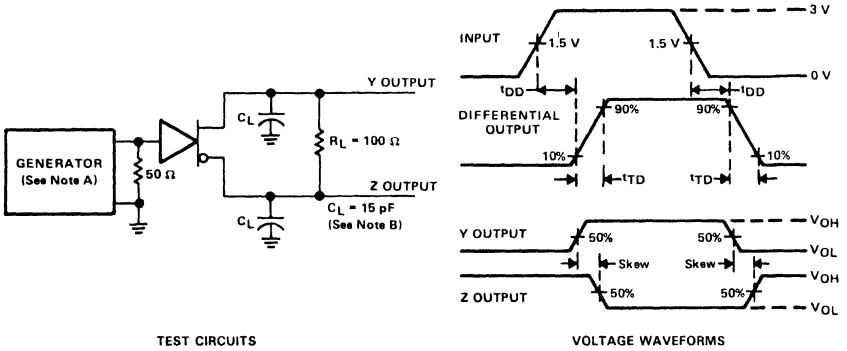


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



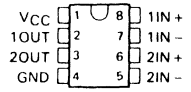
TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line and "Small Outline" Packages
- Designed to be Interchangeable with Fairchild μA9639AC

D, JG, OR P PACKAGE
(TOP VIEW)

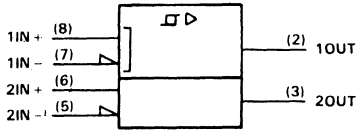


description

The uA9639C is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and "small outline" package.

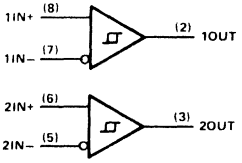
The uA9639C is characterized for operation from 0°C to 70°C.

logic symbol†

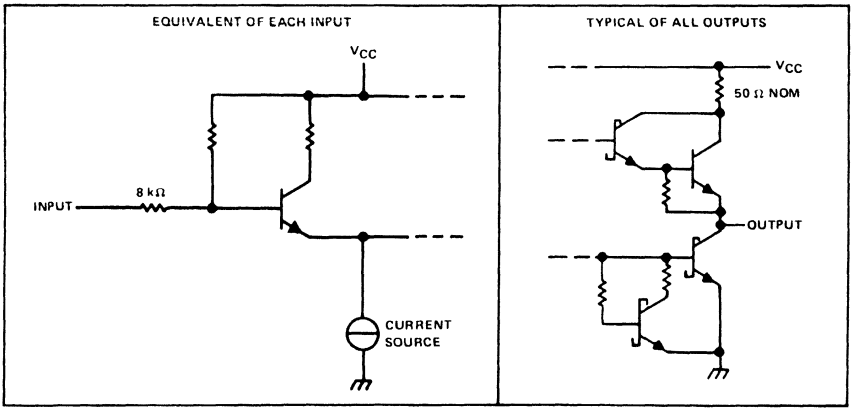


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C; and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

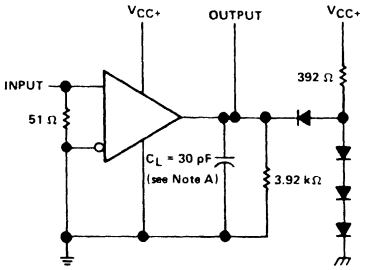
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 4. The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

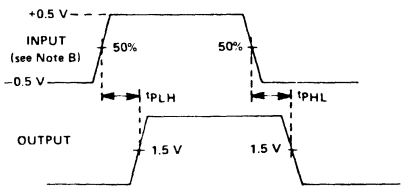
switching characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		85	ns
t_{PHL}	Propagation delay time, high-to-low-level output			85	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

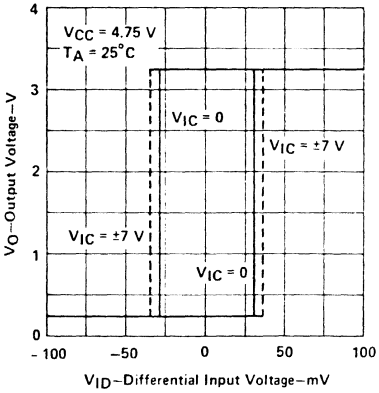


FIGURE 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

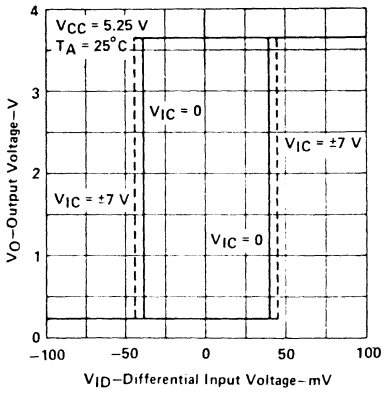


FIGURE 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

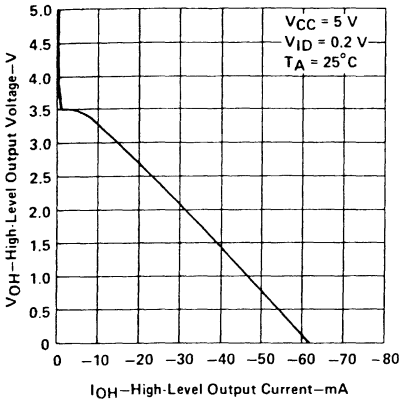


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

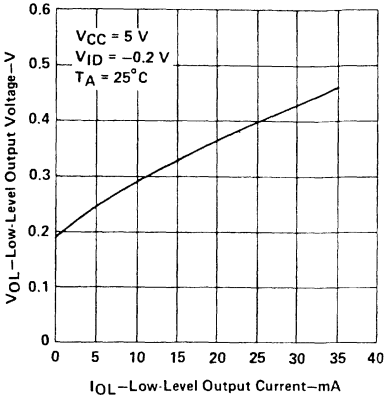


FIGURE 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

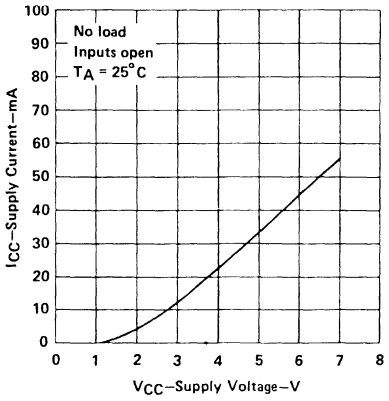


FIGURE 6

TYPICAL APPLICATION DATA

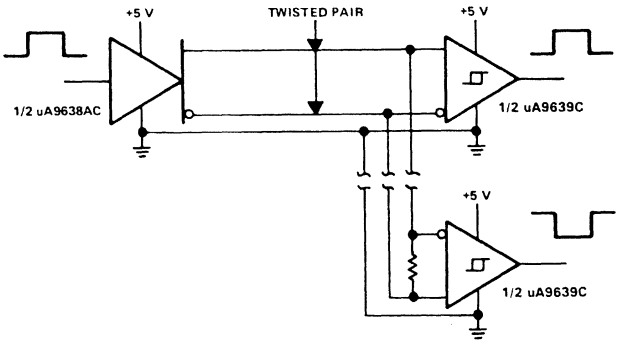


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

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